

MS-7788 Ver: 1.0 u-ATX : 226 * 173 mm

CPU:

Intel - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH(H61)

OnBoard Chipset:

HD Audio Codec:ALC887VD / VT1708SCE

LAN:RTL 8105E 10/100 , Co-lay 8111E 10/100/1000

SIO:FIN71868AD

Flash ROM: 32Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 1

PWM:

Controller: UT501 3+1 Phase

CPU+GPU: UP6282 MOSFET Driver

CPU VTT: UP1504

CPU SA : OP+MOS

DDR: UP1504

PCH: OP+MOS

ACPI:

UPI

Other:

SATA2.0 x4 (PCH)

USB2.0 RearX6 Front x4

D-SUB/DVI*1

TPM Header *1

Speaker Pin Header

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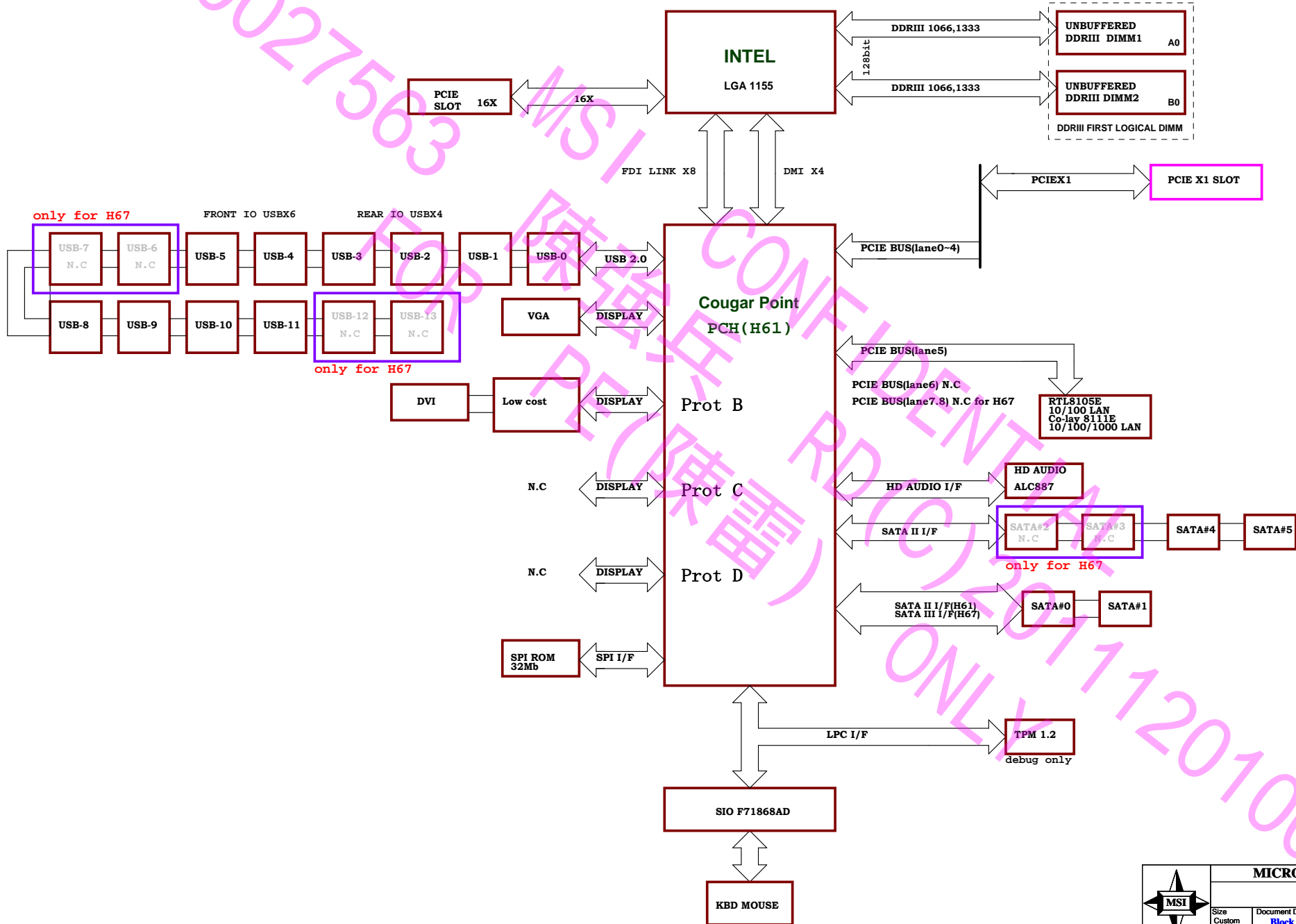
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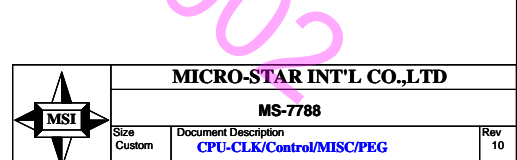
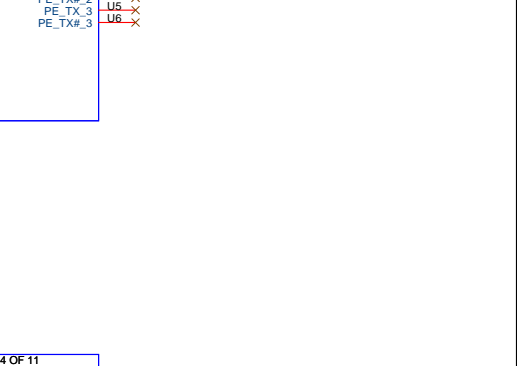
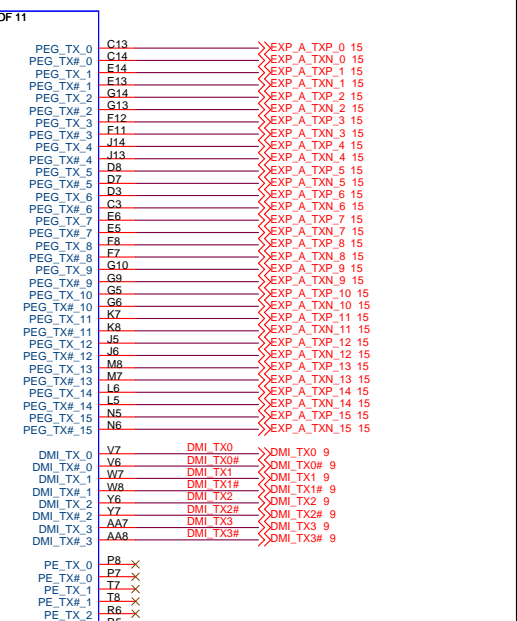
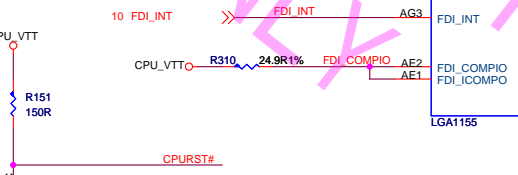
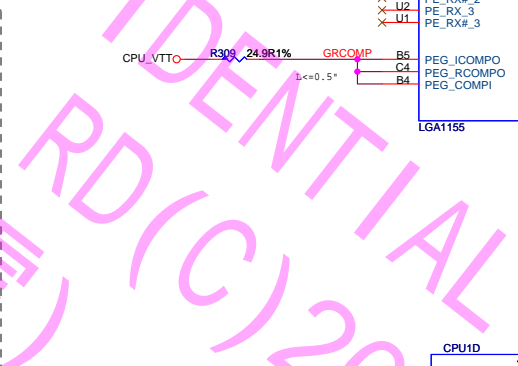
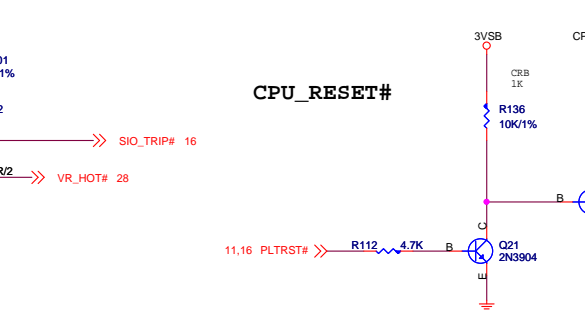
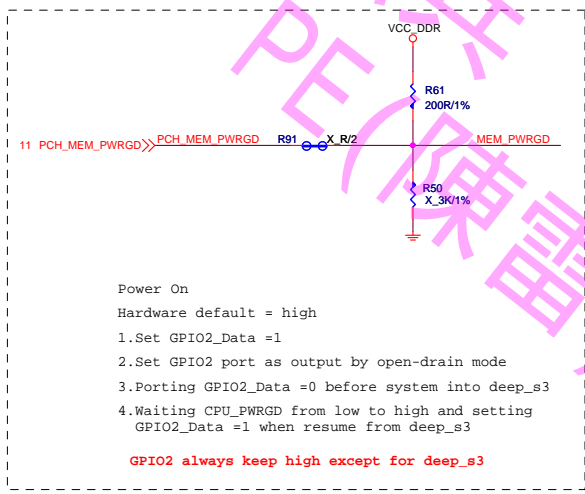
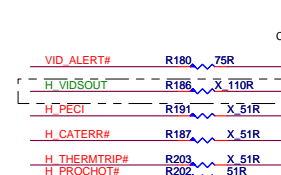
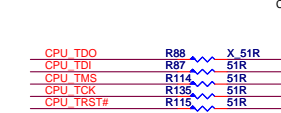
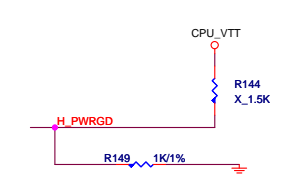
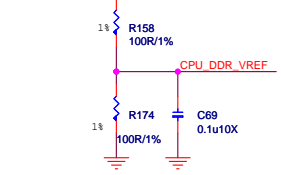
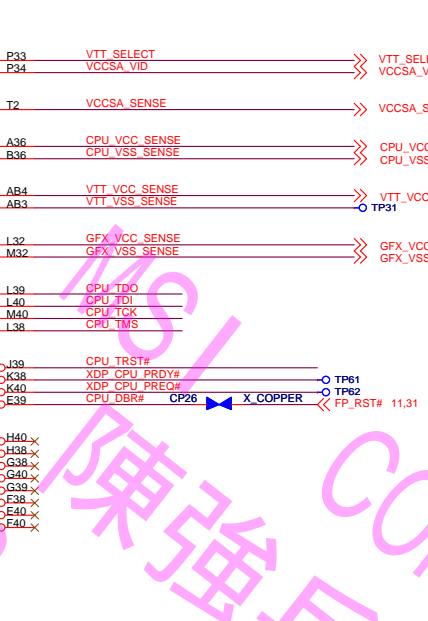
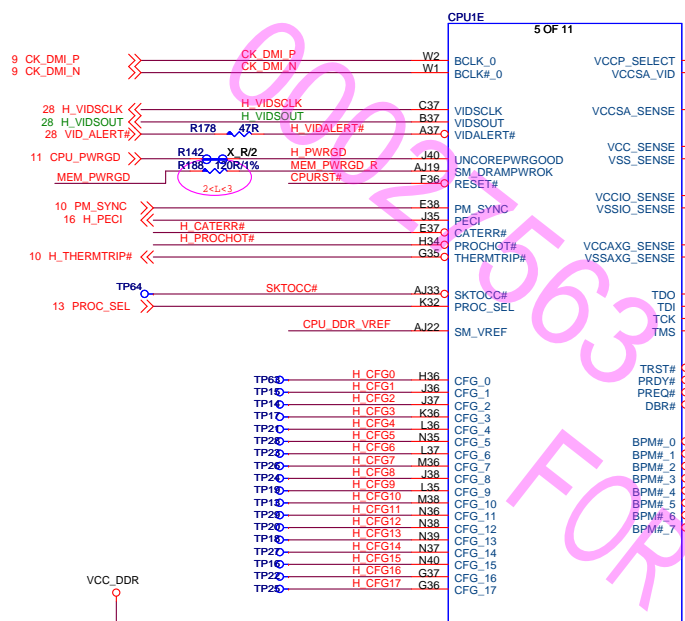
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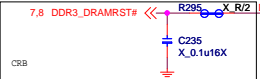
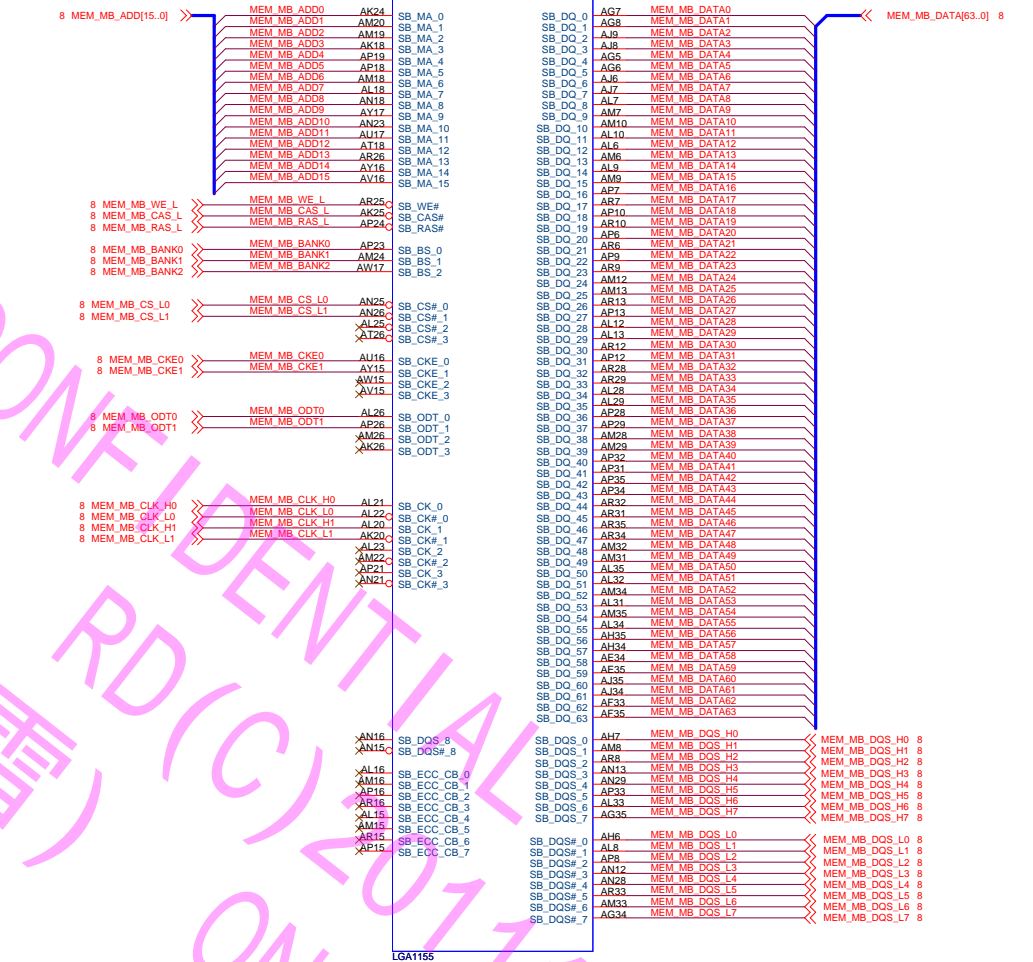
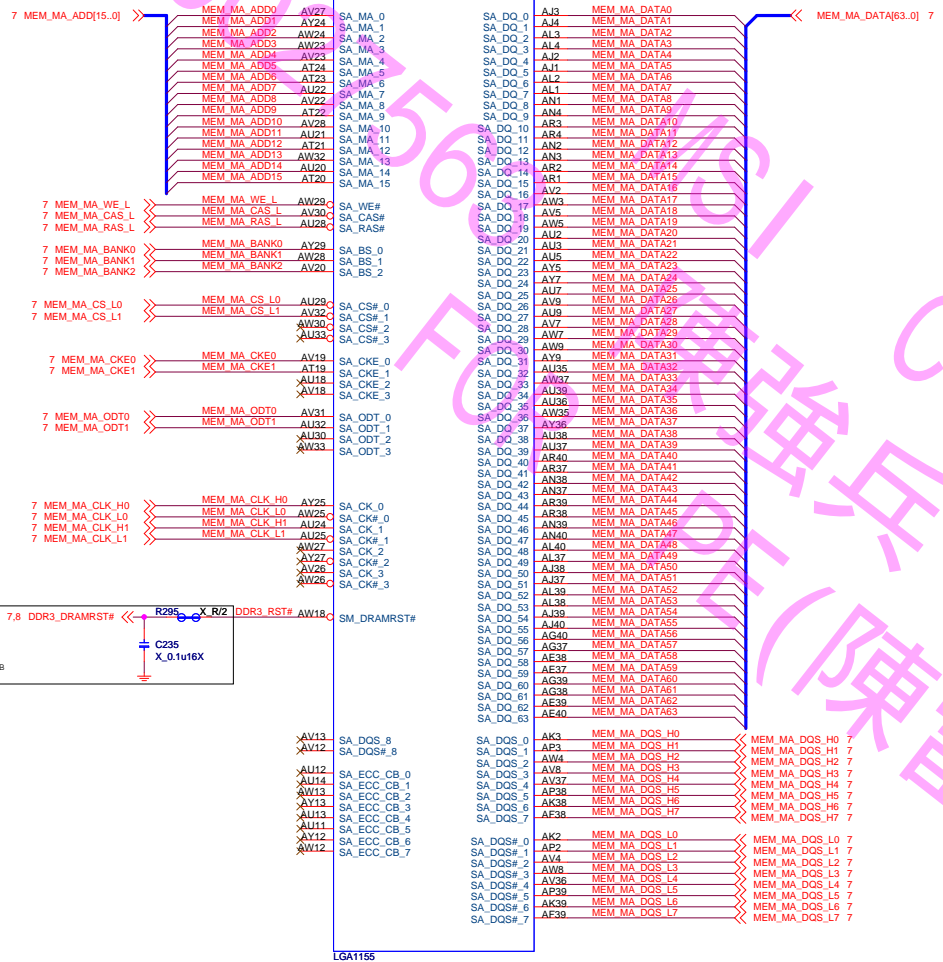




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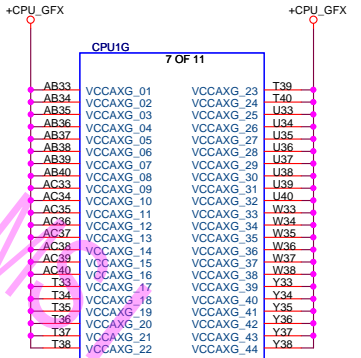
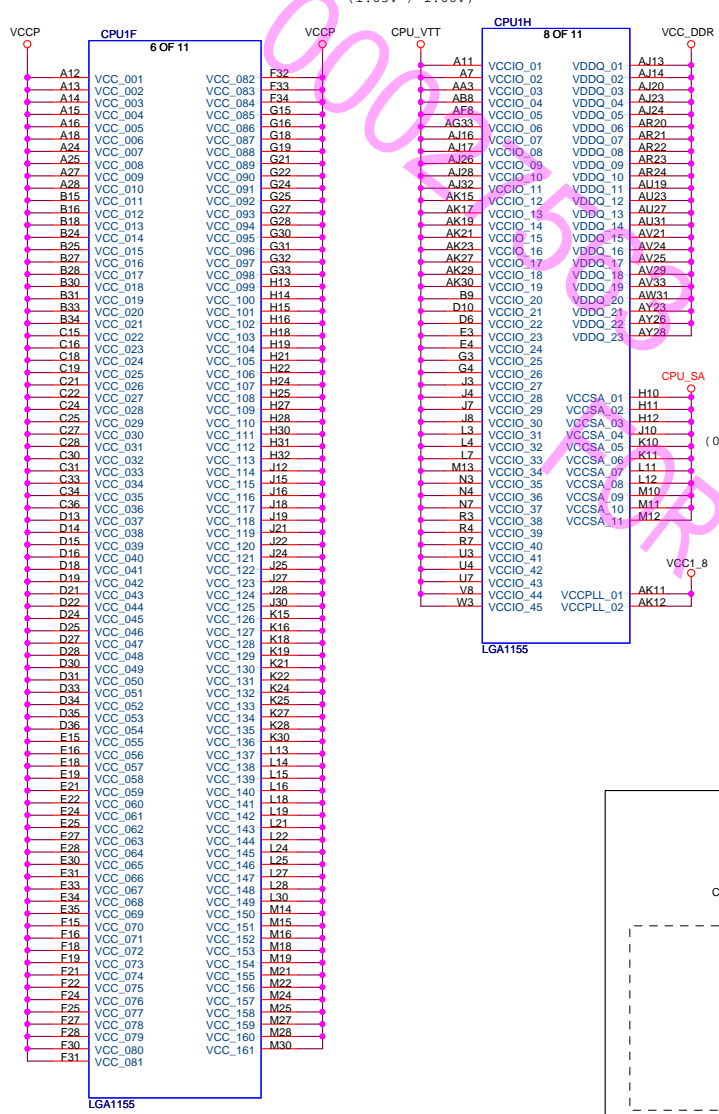
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Size: Custom Document Description: CPU-Memory Rev: 10

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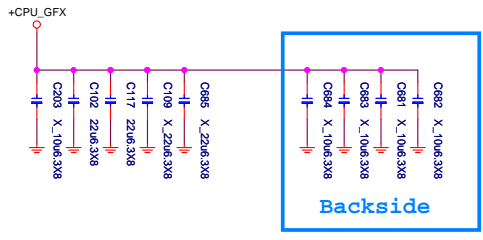
(1.05V / 1.00V)



(0.925V / 0.85V)

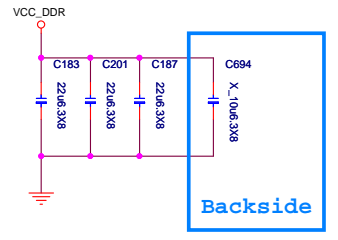
VCCP: 112A
 CPU_VTT: 8.2A
 CPU_SA: 8.8A
 VCC_DDR: 4.5A
 VCC1_8: 1.6A

+CPU_GFX Decoupling

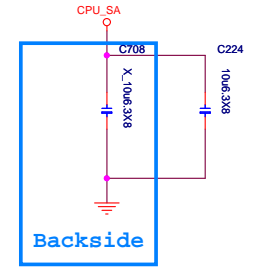


CPU SOCKET CAVITY CAPS

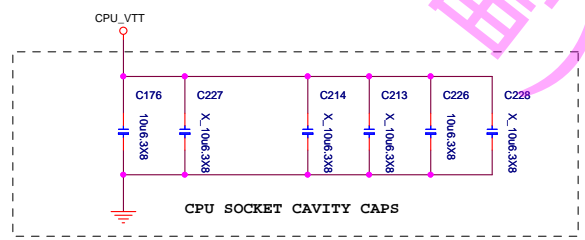
+1.5V_DDR3-Decoupling



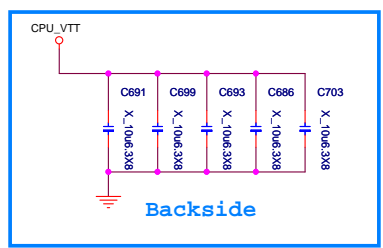
CPU SOCKET CAVITY CAPS



+CPU_VTT Decoupling

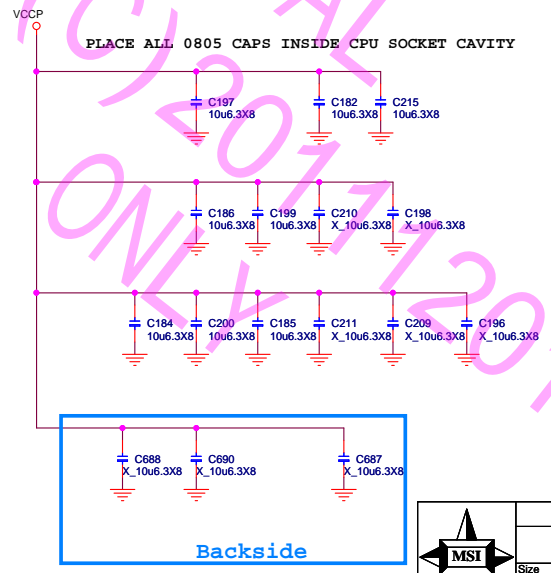


CPU SOCKET CAVITY CAPS



Backside

+CPU_VCCP-Decoupling



PLACE ALL 0805 CAPS INSIDE CPU SOCKET CAVITY

Backside



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A17	VSS_001	VSS_091	AM27
A23	VSS_002	VSS_092	AM5
A26	VSS_003	VSS_093	AM30
A29	VSS_004	VSS_094	AM36
A35	VSS_005	VSS_095	AM37
AA33	VSS_006	VSS_096	AM38
AA34	VSS_007	VSS_097	AM4
AA35	VSS_008	VSS_098	AM40
AA36	VSS_009	VSS_099	AM5
AA37	VSS_010	VSS_100	AM6
AA38	VSS_011	VSS_101	AN11
AA6	VSS_012	VSS_102	AN14
AB5	VSS_013	VSS_103	AN17
AC1	VSS_014	VSS_104	AN19
AC6	VSS_015	VSS_105	AN22
AD33	VSS_016	VSS_106	AN24
AD36	VSS_017	VSS_107	AN27
AD38	VSS_018	VSS_108	AN30
AD39	VSS_019	VSS_109	AN31
AD5	VSS_020	VSS_110	AN32
AD8	VSS_021	VSS_111	AN33
AE3	VSS_022	VSS_112	AN34
AE33	VSS_023	VSS_113	AN35
AE34	VSS_024	VSS_114	AN36
AF1	VSS_025	VSS_115	AN5
AF34	VSS_026	VSS_116	AN6
AF36	VSS_027	VSS_117	AN7
AF37	VSS_028	VSS_118	AN9
AF40	VSS_029	VSS_119	AN9
AF5	VSS_030	VSS_120	AP1
AF6	VSS_031	VSS_121	AP11
AF7	VSS_032	VSS_122	AP15
AG36	VSS_033	VSS_123	AP17
AH2	VSS_034	VSS_124	AP22
AH3	VSS_035	VSS_125	AP25
AH33	VSS_036	VSS_126	AP27
AH36	VSS_037	VSS_127	AP30
AH37	VSS_038	VSS_128	AP36
AH38	VSS_039	VSS_129	AP37
AH39	VSS_040	VSS_130	AP4
AH40	VSS_041	VSS_131	AP4
AH5	VSS_042	VSS_132	AP5
AH8	VSS_043	VSS_133	AR11
AJ12	VSS_044	VSS_134	AR14
AJ15	VSS_045	VSS_135	AR17
AJ18	VSS_046	VSS_136	AR18
AJ21	VSS_047	VSS_137	AR19
AJ25	VSS_048	VSS_138	AR27
AJ27	VSS_049	VSS_139	AR30
AJ36	VSS_050	VSS_140	AR36
AJ5	VSS_051	VSS_141	AR5
AK5	VSS_052	VSS_142	AT1
AK1	VSS_053	VSS_143	AT10
AK10	VSS_054	VSS_144	AT12
AK13	VSS_055	VSS_145	AT13
AK14	VSS_056	VSS_146	AT15
AK16	VSS_057	VSS_147	AT16
AK22	VSS_058	VSS_148	AT17
AK28	VSS_059	VSS_149	AT2
AK31	VSS_060	VSS_150	AT25
AK32	VSS_061	VSS_151	AT27
AK33	VSS_062	VSS_152	AT28
AK34	VSS_063	VSS_153	AT29
AK35	VSS_064	VSS_154	AT3
AK36	VSS_065	VSS_155	AT30
AK37	VSS_066	VSS_156	AT31
AK4	VSS_067	VSS_157	AT32
AK40	VSS_068	VSS_158	AT33
AK5	VSS_069	VSS_159	AT34
AK6	VSS_070	VSS_160	AT35
AK7	VSS_071	VSS_161	AT36
AK8	VSS_072	VSS_162	AT37
AK9	VSS_073	VSS_163	AT38
AL11	VSS_074	VSS_164	AT39
AL14	VSS_075	VSS_165	AT4
AL17	VSS_076	VSS_166	AT5
AL19	VSS_077	VSS_167	AT6
AL24	VSS_078	VSS_168	AT7
AL27	VSS_079	VSS_169	AT8
AL30	VSS_080	VSS_170	AT9
AL36	VSS_081	VSS_171	G20
AL5	VSS_082	VSS_172	G21
AM1	VSS_083	VSS_173	G22
AM11	VSS_084	VSS_174	G23
AM14	VSS_085	VSS_175	G26
AM17	VSS_086	VSS_176	G29
AM2	VSS_087	VSS_177	G34
AM21	VSS_088	VSS_178	G7
AM23	VSS_089	VSS_179	G8
AM25	VSS_090	VSS_180	G11

LGA1155

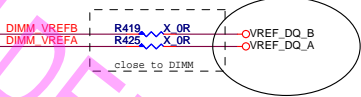
CPU1J
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AV11	VSS_181	VSS_281	H37
AV14	VSS_182	VSS_282	H39
AV17	VSS_183	VSS_283	H5
AV3	VSS_184	VSS_284	H6
AV35	VSS_185	VSS_285	H9
AV38	VSS_186	VSS_286	J11
AV6	VSS_187	VSS_287	J17
AW10	VSS_188	VSS_288	J20
AW11	VSS_189	VSS_289	J23
AW14	VSS_190	VSS_290	J26
AW16	VSS_191	VSS_291	J29
AW36	VSS_192	VSS_292	J32
AW6	VSS_193	VSS_293	K1
AY11	VSS_194	VSS_294	K12
AY14	VSS_195	VSS_295	K13
AY17	VSS_196	VSS_296	K14
AY35	VSS_197	VSS_297	K17
AYA	VSS_198	VSS_298	K2
AY6	VSS_199	VSS_299	K20
AY8	VSS_200	VSS_300	K23
B10	VSS_201	VSS_301	K26
B13	VSS_202	VSS_302	K29
B14	VSS_203	VSS_303	K33
B17	VSS_204	VSS_304	K35
B23	VSS_205	VSS_305	K37
B26	VSS_206	VSS_306	K39
B29	VSS_207	VSS_307	K5
B32	VSS_208	VSS_308	K6
B35	VSS_209	VSS_309	L10
B38	VSS_210	VSS_310	L17
B6	VSS_211	VSS_311	L20
C11	VSS_212	VSS_312	L23
C12	VSS_213	VSS_313	L26
C17	VSS_214	VSS_314	L29
C14	VSS_215	VSS_315	LA
C23	VSS_216	VSS_316	M1
C26	VSS_217	VSS_317	M17
C29	VSS_218	VSS_318	M2
C32	VSS_219	VSS_319	M20
C30	VSS_220	VSS_320	M26
CP36	VSS_221	VSS_321	M29
C7	VSS_222	VSS_322	M33
C8	VSS_223	VSS_323	M39
D17	VSS_224	VSS_324	M37
D2	VSS_225	VSS_325	M39
D20	VSS_226	VSS_326	M39
D23	VSS_227	VSS_327	M5
D26	VSS_228	VSS_328	M6
D29	VSS_229	VSS_329	M6
D32	VSS_230	VSS_330	M9
D37	VSS_231	VSS_331	N8
D39	VSS_232	VSS_332	P1
D4	VSS_233	VSS_333	P2
D5	VSS_234	VSS_334	P38
D9	VSS_235	VSS_335	P40
E11	VSS_236	VSS_336	P5
E12	VSS_237	VSS_337	P5
E17	VSS_238	VSS_338	R33
E20	VSS_239	VSS_339	R35
E23	VSS_240	VSS_340	R37
E26	VSS_241	VSS_341	R39
E29	VSS_242	VSS_342	R8
E32	VSS_243	VSS_343	T1
E36	VSS_244	VSS_344	T5
E7	VSS_245	VSS_345	T6
E8	VSS_246	VSS_346	U8
F11	VSS_247	VSS_347	V1
F10	VSS_248	VSS_348	V2
F13	VSS_249	VSS_349	V33
F14	VSS_250	VSS_350	V34
F17	VSS_251	VSS_351	V35
F2	VSS_252	VSS_352	V36
F23	VSS_253	VSS_353	V37
F26	VSS_254	VSS_354	V38
F29	VSS_255	VSS_355	V40
F35	VSS_256	VSS_356	V5
F37	VSS_257	VSS_357	V6
F39	VSS_258	VSS_358	V5
F5	VSS_259	VSS_359	V8
F6	VSS_260	VSS_360	V8
F9	VSS_261		
G11	VSS_262		
G12	VSS_263		
G17	VSS_264		
G20	VSS_265		
G23	VSS_266		
G26	VSS_267		
G29	VSS_268		
G34	VSS_269		
G7	VSS_270		
G8	VSS_271		
H1	VSS_272		
H17	VSS_273	VSS_NCTF_01	A4
H2	VSS_274	VSS_NCTF_02	AV39
H20	VSS_275	VSS_NCTF_03	AY37
H23	VSS_276	VSS_NCTF_04	B3
H26	VSS_277		
H29	VSS_278		
H33	VSS_279		
H35	VSS_280		

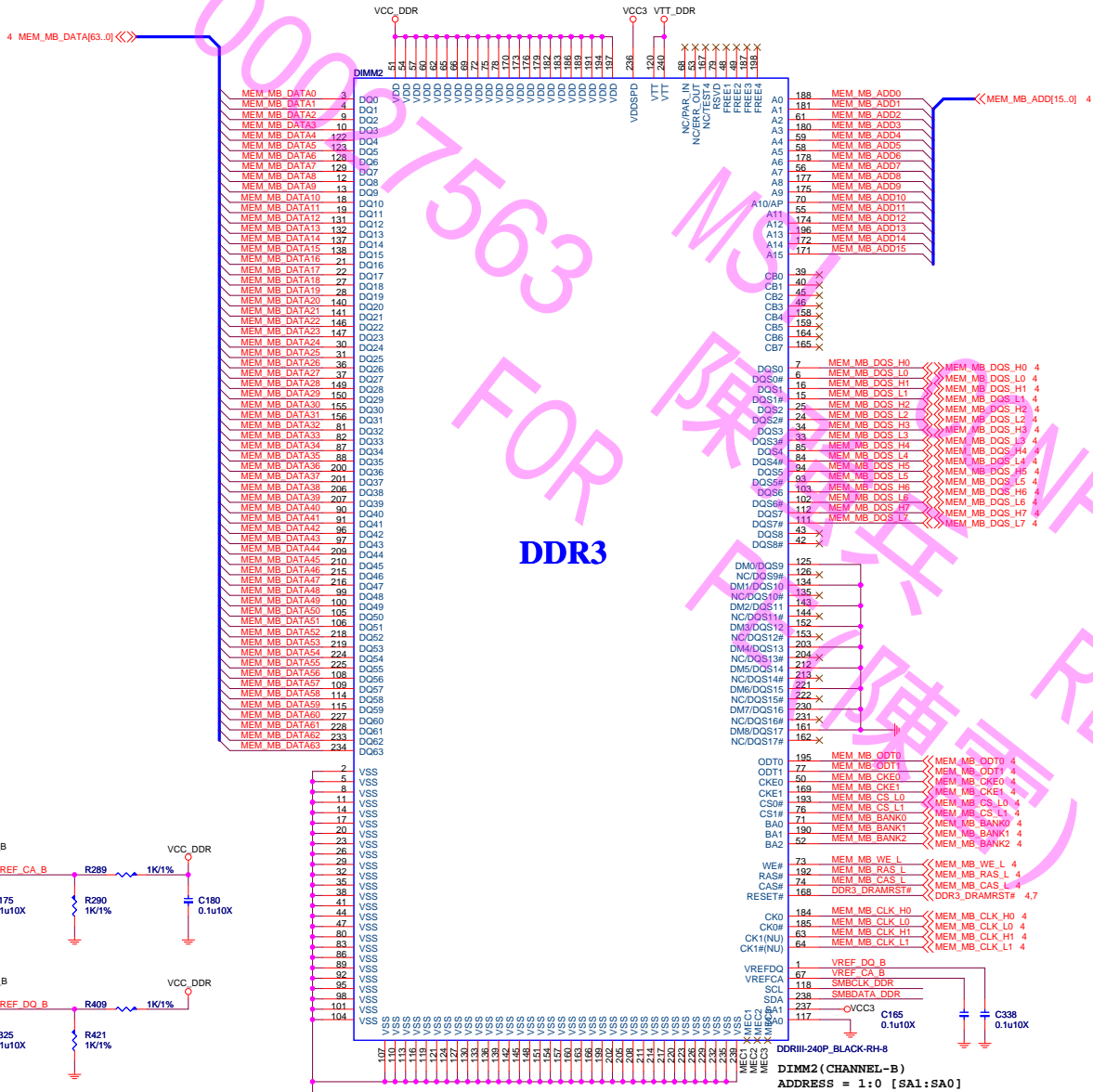
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CPU1K
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C40	RSVD_001	RSVD_036	L33
D40	RSVD_002	RSVD_037	L34
AB6	RSVD_003	RSVD_038	M34
AB7	RSVD_004	RSVD_039	N33
AD37	RSVD_005	RSVD_040	N34
AE6	RSVD_006	RSVD_041	P45
AG4	RSVD_007	RSVD_043	P37
AI11	RSVD_008	RSVD_044	P39
AI29	RSVD_009	RSVD_045	R34
AI30	RSVD_010	RSVD_046	R36
AI31	RSVD_011	RSVD_047	R38
AI31	RSVD_012	RSVD_048	R40
AN20	RSVD_013	RSVD_049	J31
AT11	RSVD_014	RSVD_050	AD34
AT14	RSVD_015	RSVD_051	AD35
AI10	RSVD_016	RSVD_052	K31
AV1	RSVD_017	RSVD_053	
AV34	RSVD_018		
AW2	RSVD_019		
D2	RSVD_020		
D2	RSVD_021		
AY3	RSVD_022		
AY3	RSVD_023		
B39	RSVD_024		
C38	RSVD_025		
D39	RSVD_026		
H7	RSVD_027		
H8	RSVD_028		
J33	RSVD_029		
J34	RSVD_030		
J9	RSVD_031		
K34	RSVD_032		
K9	RSVD_033		
L31	RSVD_034		
FC_AH1	NCTF_01	A38	
FC_AH4	NCTF_02	AU40	
	NCTF_03	AW38	
	NCTF_04	C2	
	NCTF_05	D1	



DDRIII DIMM_B0

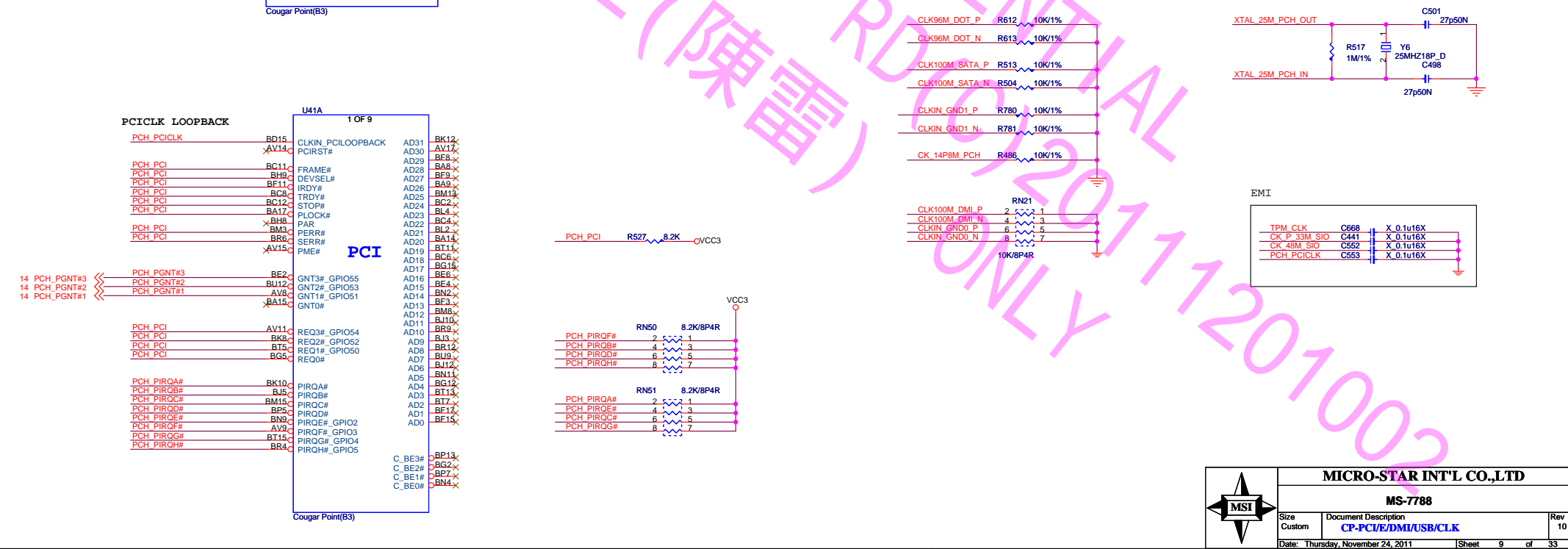
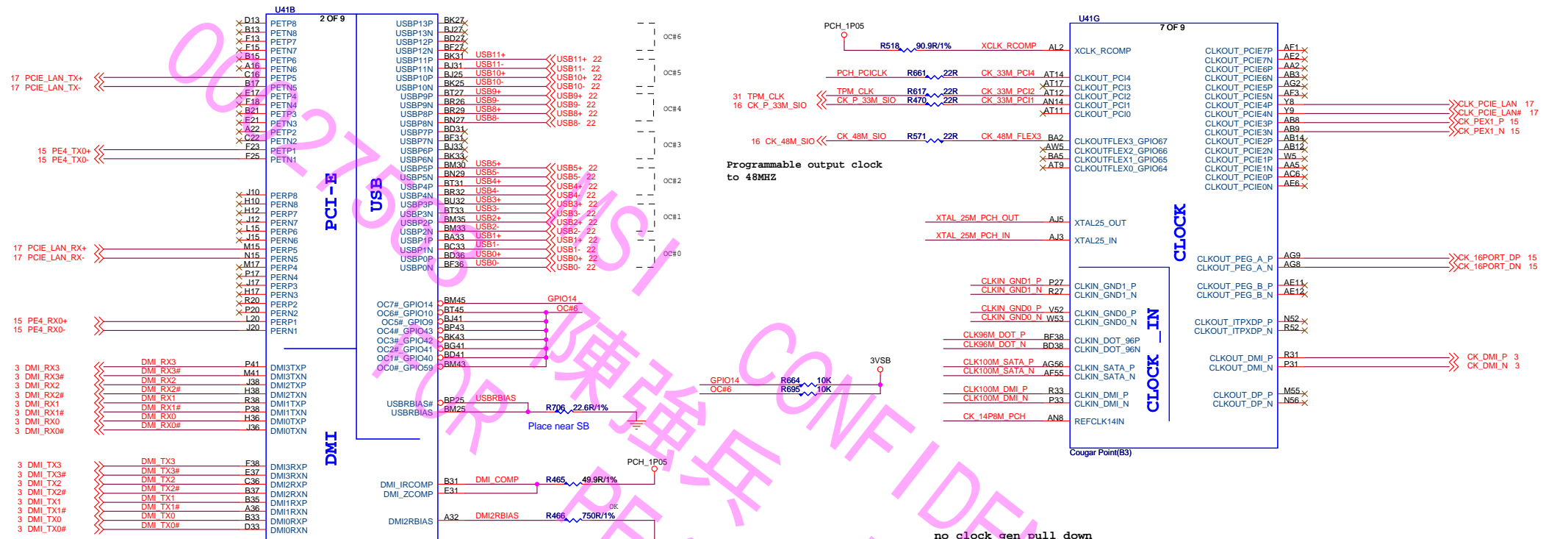


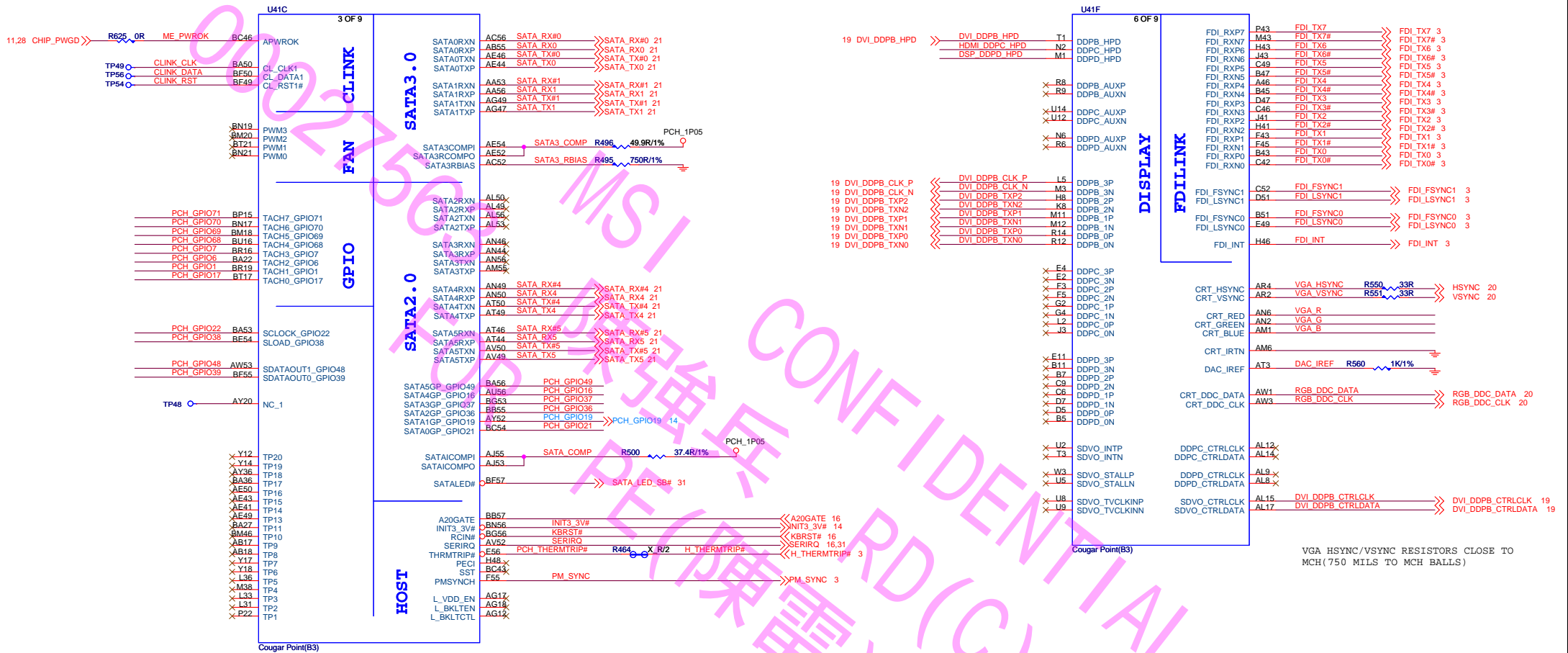
DDR3

DDRIII-240P_BLACK-RH-8
DIMM2 (CHANNEL-B)
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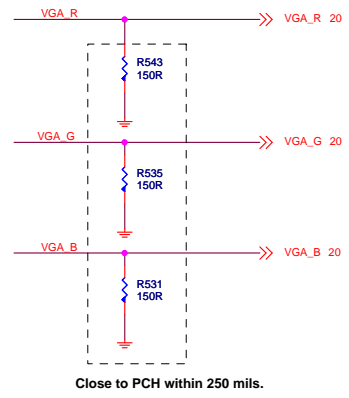
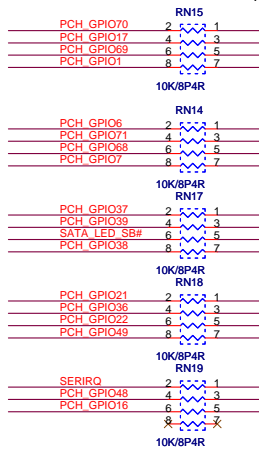
SBMCLK_DDR << SBMCLK_DDR 7
SMBDATA_DDR << SMBDATA_DDR 7

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	MS-7788	
Size Custom	Document Description DDR III DIMM 2	Rev 10
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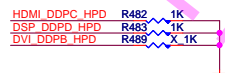




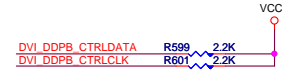
Pull HIGH for PCH



No VGA(pull down)



Enable VGA(CTRLCLK/DATA Pull High)



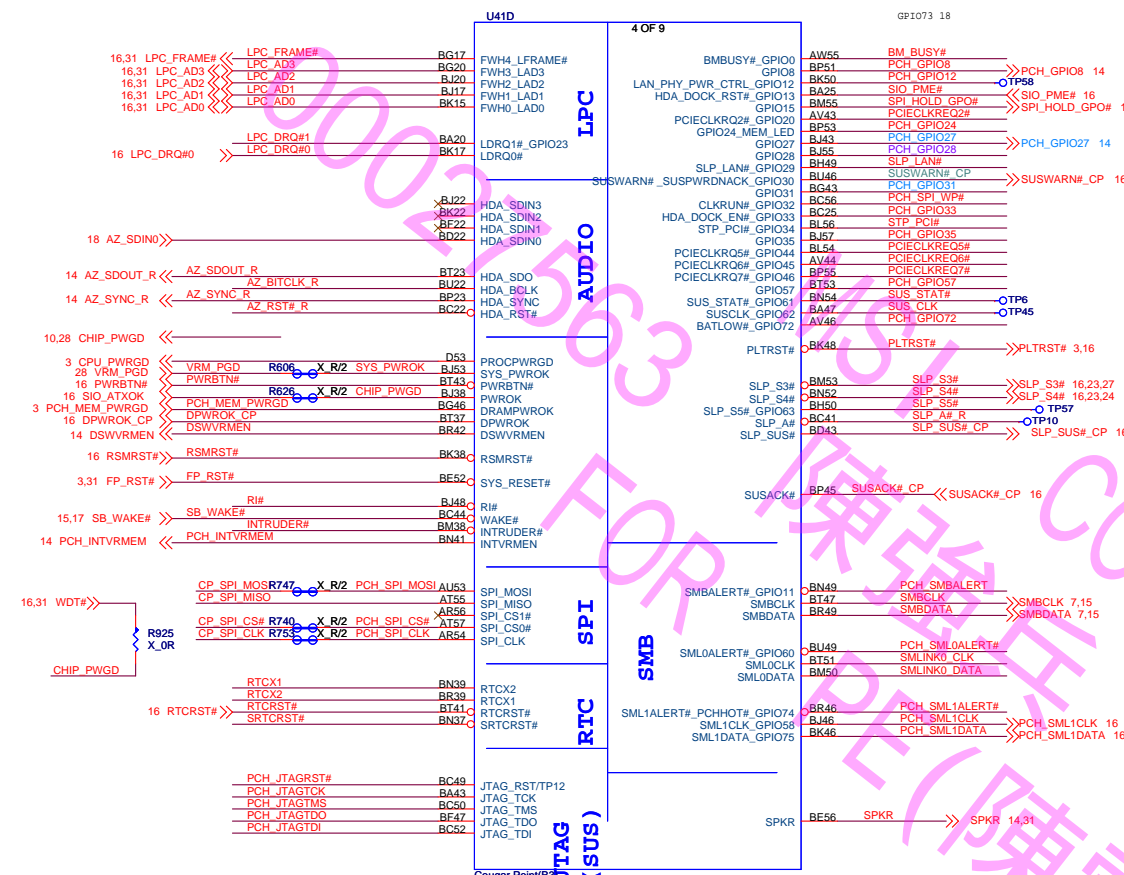
VGA HSYNC/VSYNC RESISTORS CLOSE TO MCH(750 MILS TO MCH BALLS)

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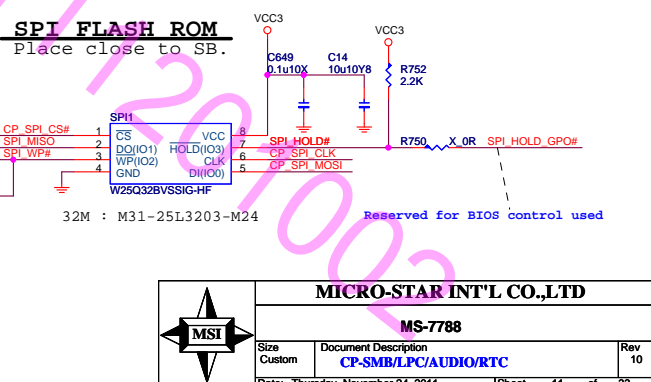
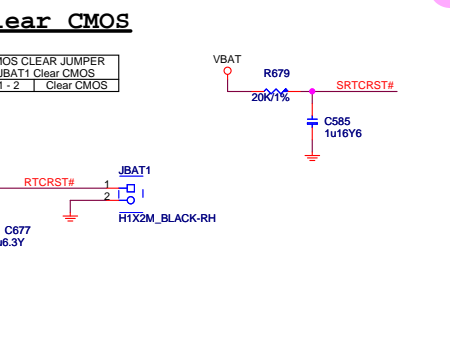
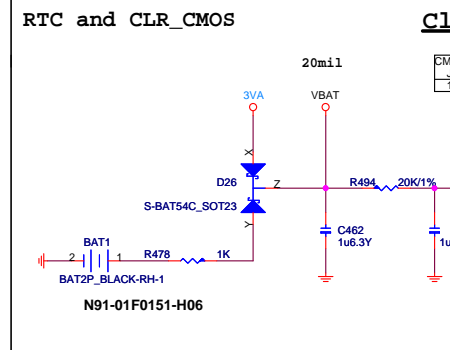
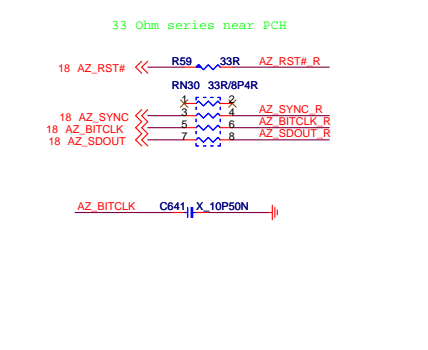
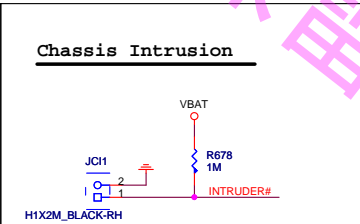
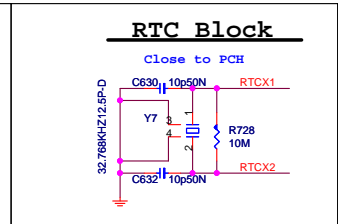
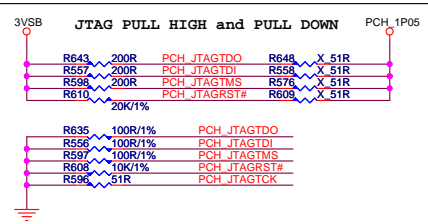
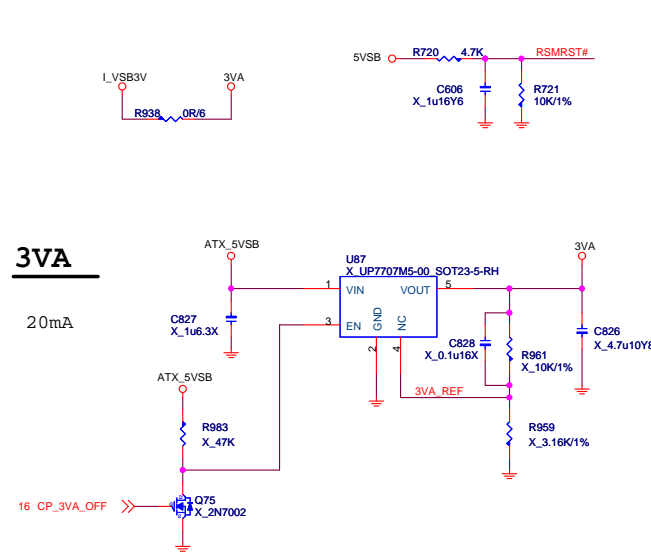
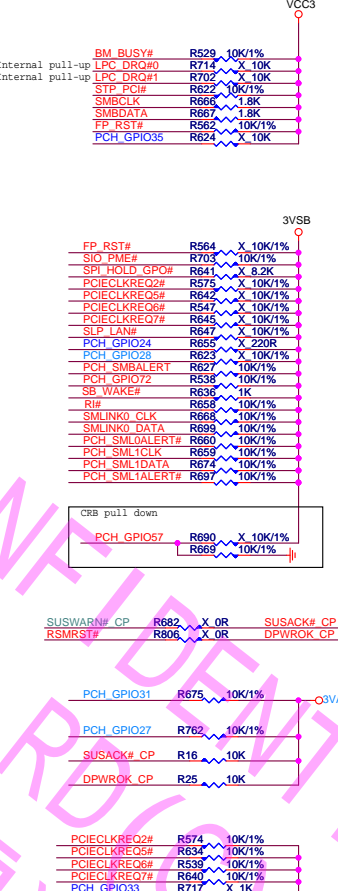
MS-7788

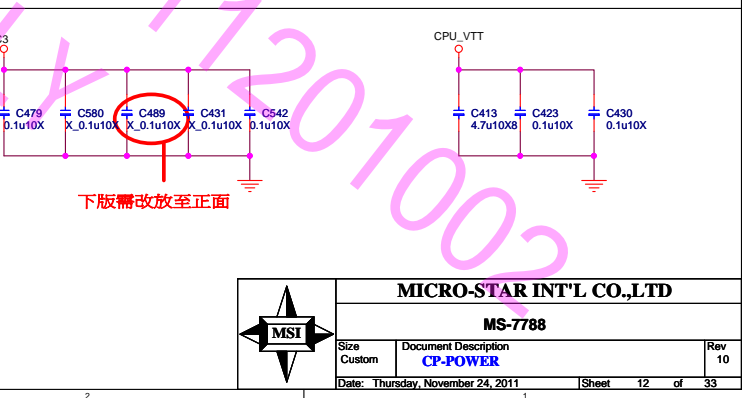
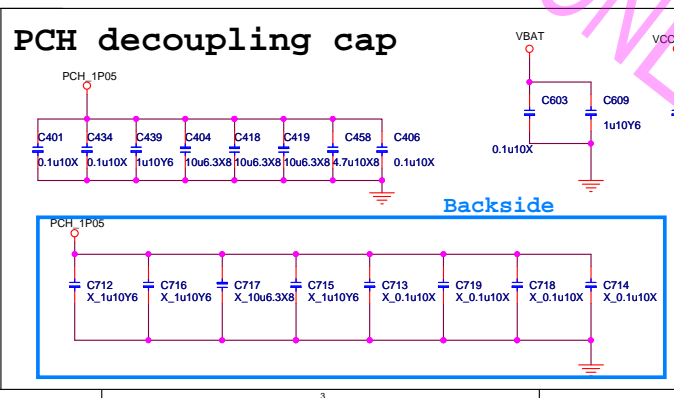
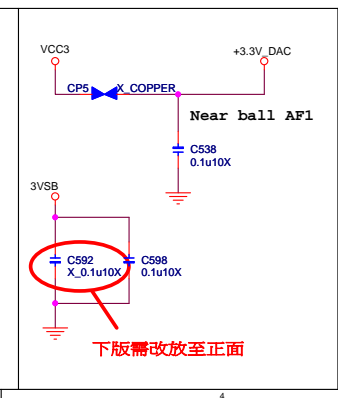
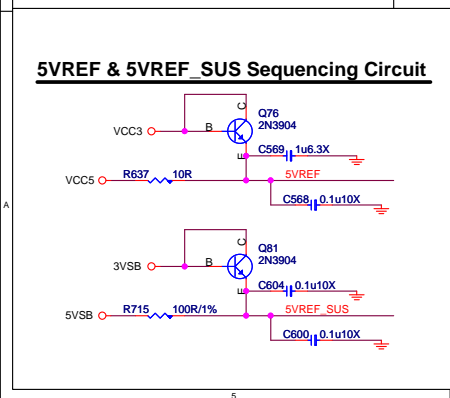
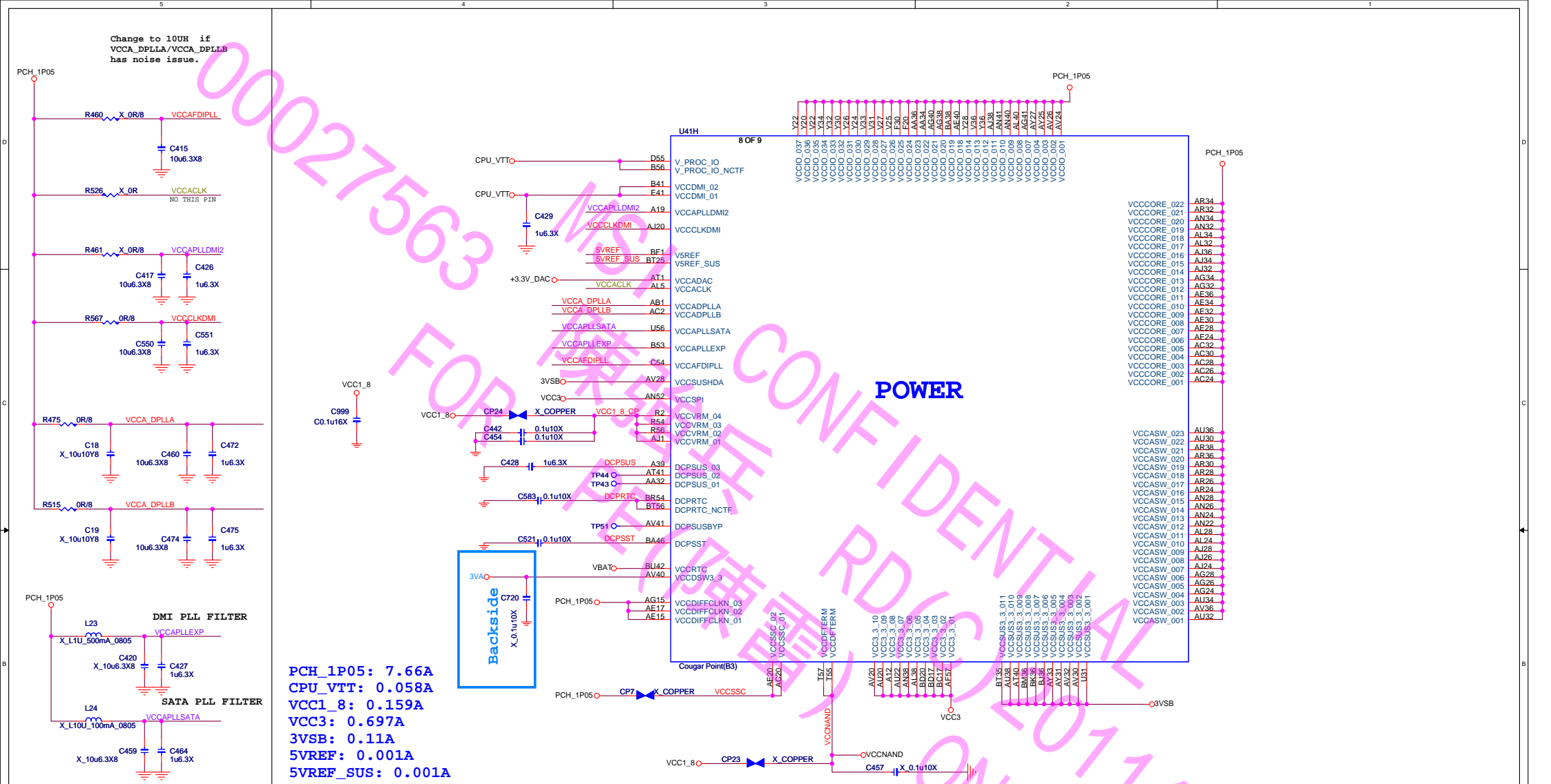
Size	Document Description	Rev
Custom	CP-SATA/HOST/FAN/GPIO/VGA	10

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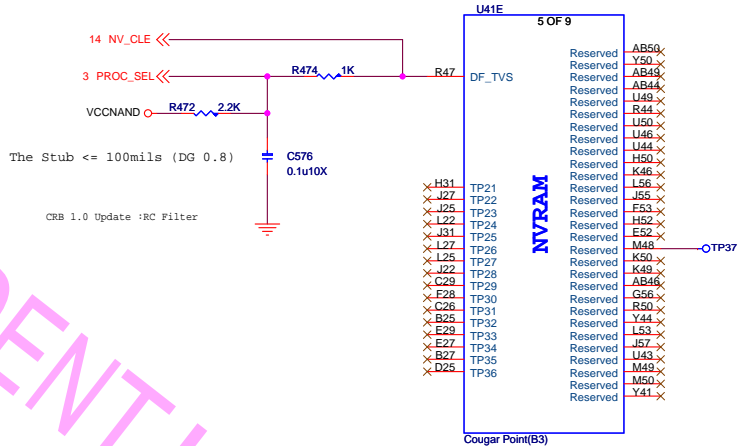


REQUIRED STRAPS





MSI		
MICRO-STAR INT'L CO.,LTD		
MS-7788		
Size Custom	Document Description CP-POWER	Rev 10
Date: Thursday, November 24, 2011	Sheet 12 of 33	



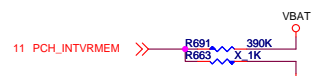
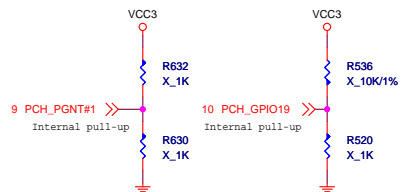
Cougar Point(B3)

Cougar Point(B3)

MICRO-STAR INT'L CO.,LTD		
MS-7788		
Size Custom	Document Description CP-GND/NVRAM	Rev 10
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PCH Straps

BOOT DEVICE	GNT1	SATALGP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



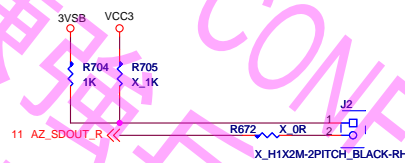
INTVRMEN
 0: DISABLE INTERNAL VRM
 1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



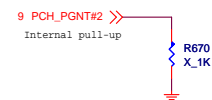
DSWVRMEN
 0 : Disable Internal Deep Sleep 1.05 V regulators.
 1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be connected even when not supporting DSW.

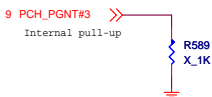


HDA_SDO
 Disable ME in Manufacturing Mode when pull LOW ????

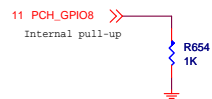
HDA_SDO has internal pull down. Default should be connected to SDIN of codec, no pull up/down. To Disable ME need to have a jumper to pull high



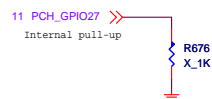
DMI AC/DC MODE
 0 : AC
 1 : DC *



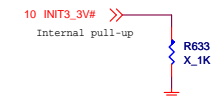
Topblock swap override when pull-low
 Signal has a weak internal pull-up



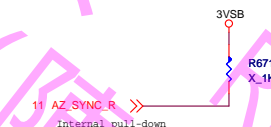
GPIO8
 0 : Integrated Clocking Enable (FCIM) *
 1 : Buffer Through Mode Enable (BTM)



GPIO28
 0 : OD PLL VR disabled
 1 : OD PLL VR enabled *
 Signal has a weak internal pull-up



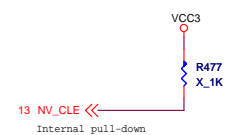
INIT3_3V#
 0 : ??????????????????
 1 : ?????????????????? *



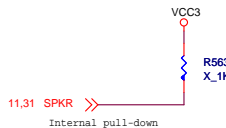
HDA_SYNC
 OD PLL VR SUPPLY SEL
 0 : 1.8V SUPPLY *
 1 : 1.5V SUPPLY



GPIO15
 0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
 1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE
 DC COUPLED: TX/RX TO VCC IF SAMPLED HIGH
 DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
 AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



SPKR
 0 : EN TCO REBOOT *
 1 : DIS TCO REBOOT

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
 0: Can not to reset the processor.

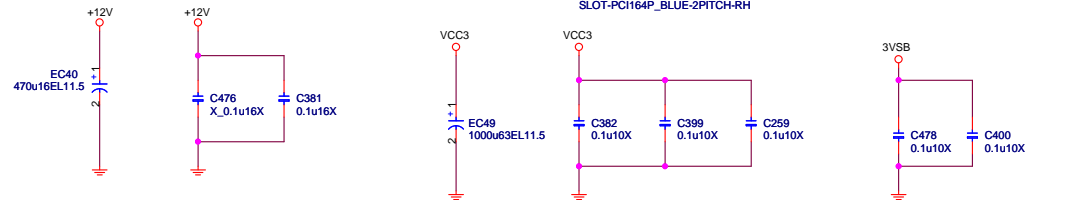
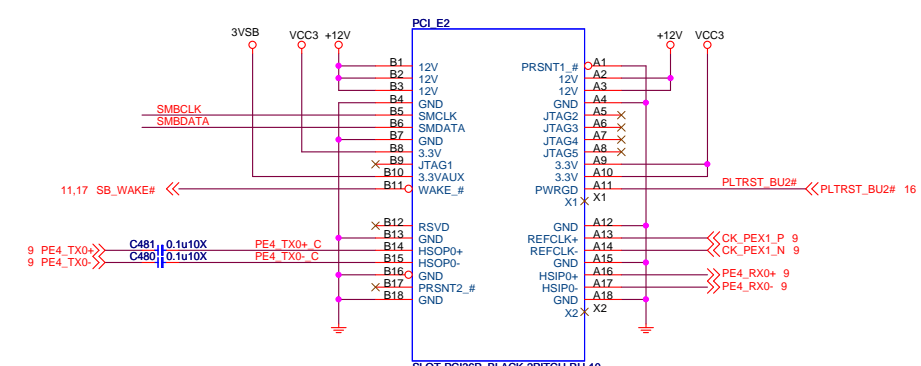
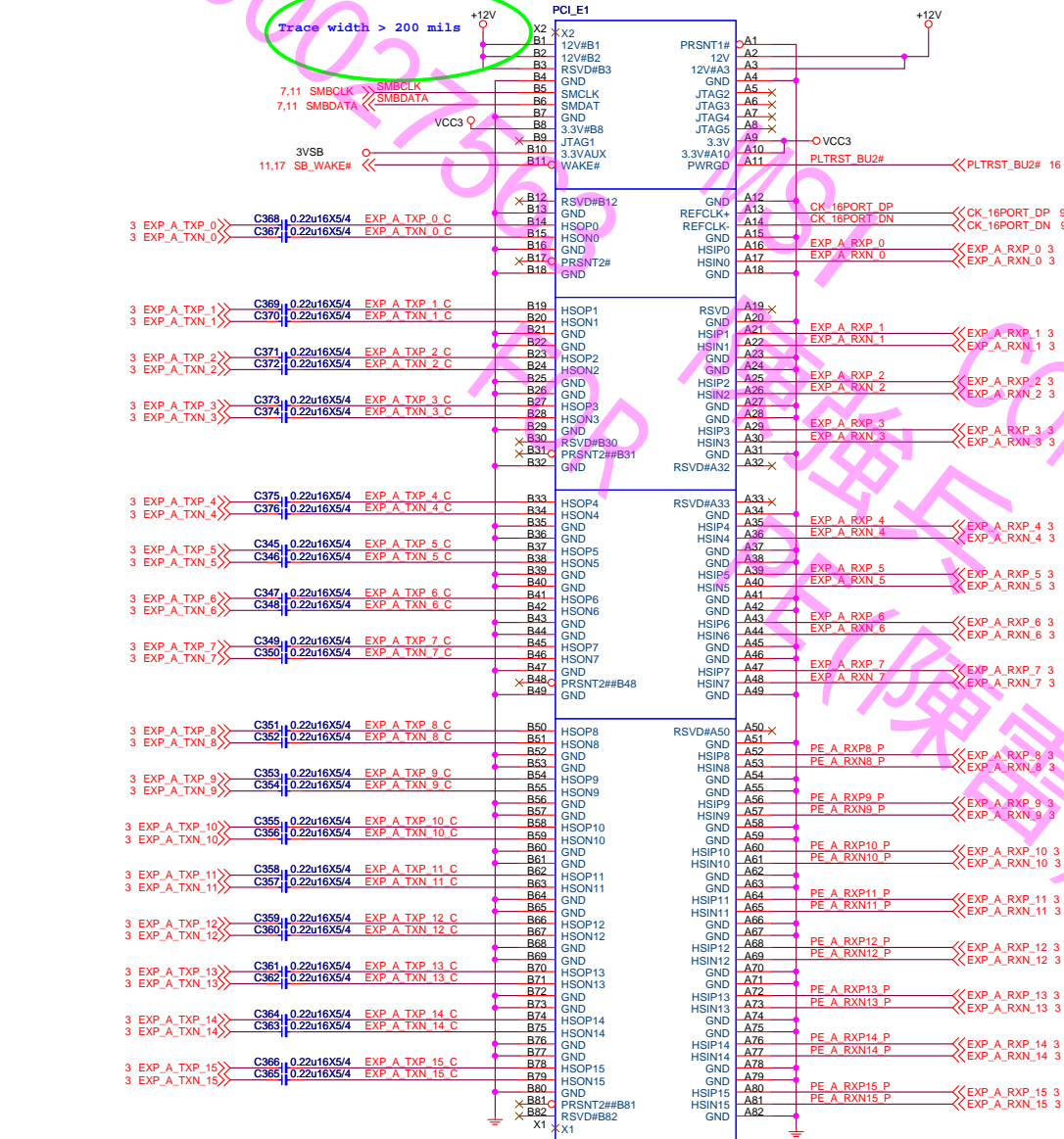
MICRO-STAR INT'L CO.,LTD		
MS-7788		
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PCI_Express X16 slot

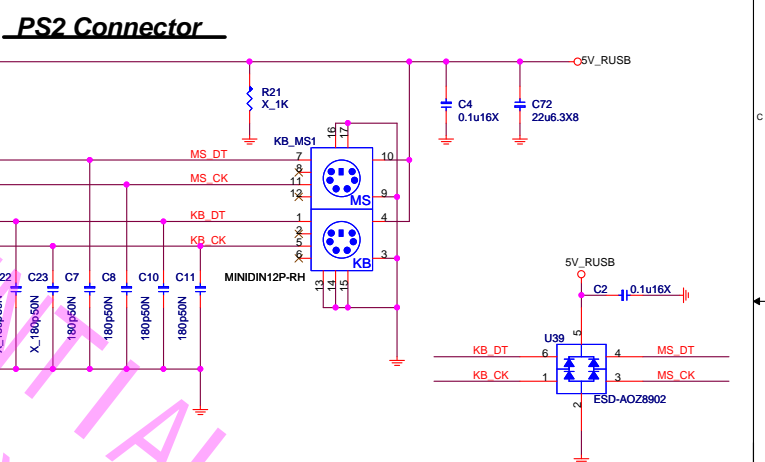
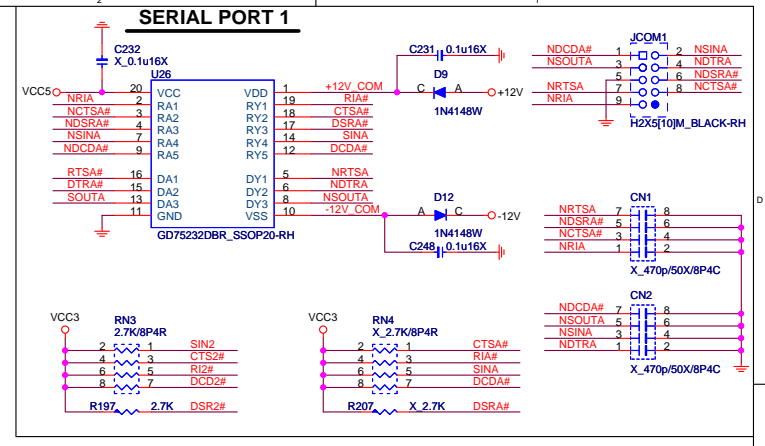
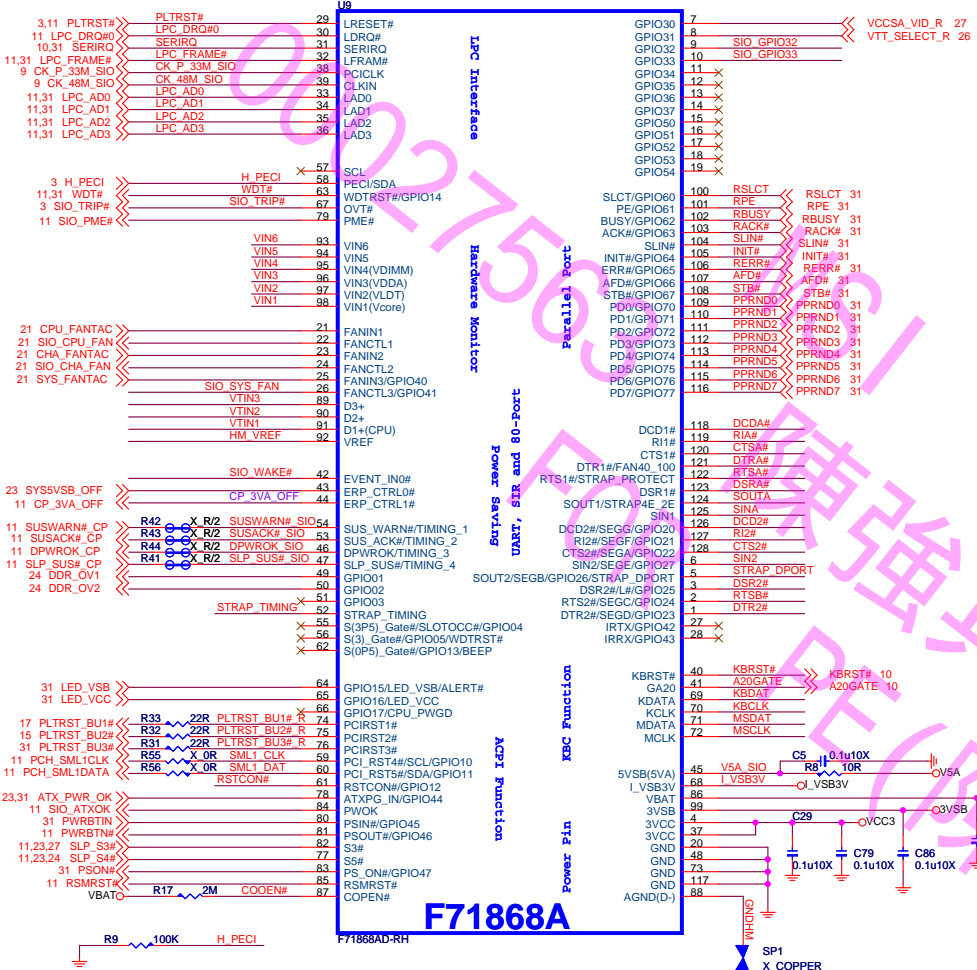
N11-1640971-K06

Trace width > 200 mils

PCI EXPRESS x1-PORT



MICRO-STAR INT'L CO.,LTD		
MS-7788		
Size Custom	Document Description PCIE x16 /x1	Rev 10
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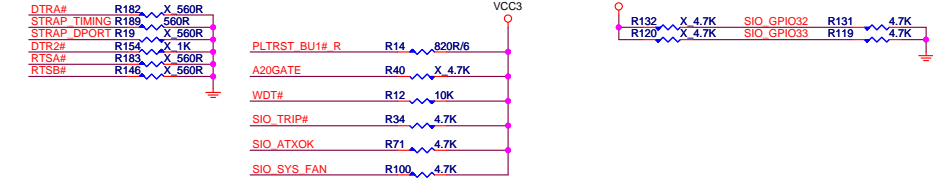
LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 40%	FAN START DUTY 100%
STRAP TIMING	AMD Timing	Intel Courgar point Timing
FANCTL 1/2/3	DAC Mode	PWM Mode
STRAP DPORT(SOUT2)	Enable 80 Port	Disable 80 Port
Strap_pectect (RTSA#)	Alarm mode	Force mode

MB ID

GPIO	32	33
SKU_A	0	0
	0	1
	1	0
	1	1

OPT BOM



HW Monitor - Thermal

HM VREF

CPU Socket

RT3 X 10KRT1%6

C74 X 2200p50X

GNDHM

HW Monitor - Voltage

VCCP R194 10K/1% VIN1

+12VIN R192 200K/1% VIN4

VCC_DDR R185 10K/1% VINS5

CPU_VTT R175 10K/1% VIN6

VCC5 R196 200K/1% VIN3

R195 47K/1%

R179 10K/1%

Close to Hot point

VTIN3

C67 2200p50X S/IO

GNDHM

VTIN2

MOS Q1

C68 X 2200p50X

GNDHM

MICRO-STAR INT'L CO.,LTD

MS-7788

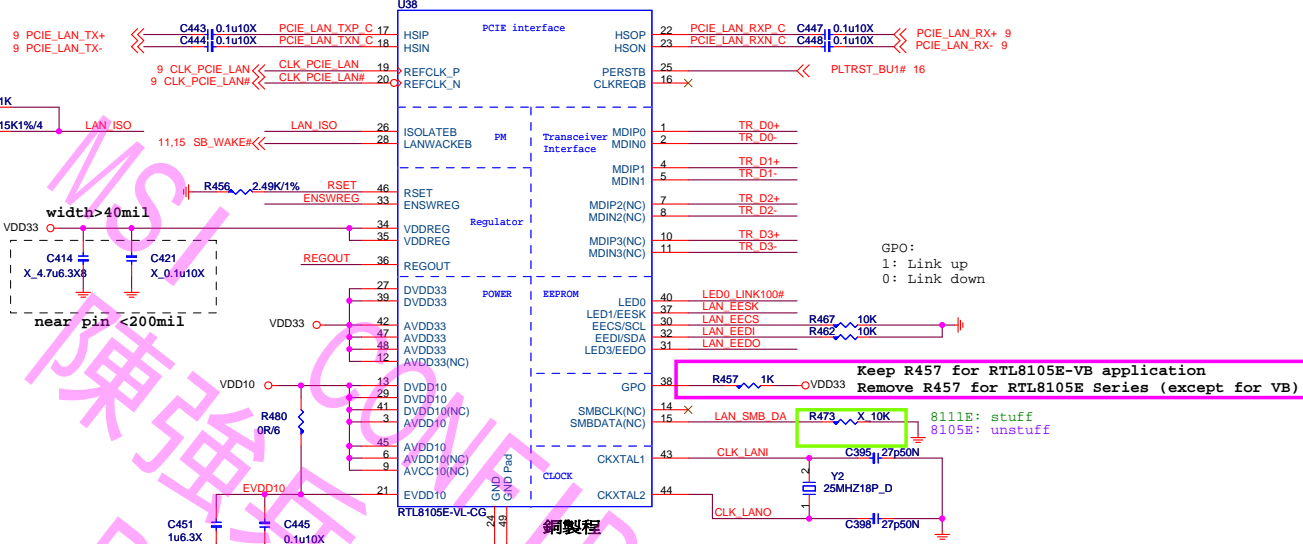
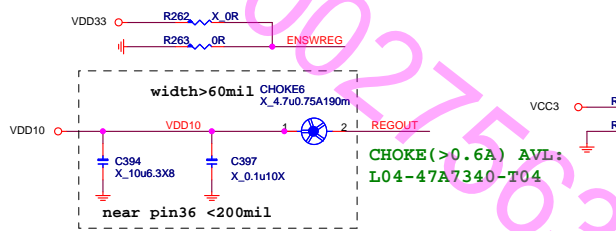
Size Custom	Document Description SIO-Fintek F71868AD(EUP)	Rev 10
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Power Regulator Option

	Mode	Choke6	C394	C397	C414	C421	R262	R263
8111E Series & 8105E Series	SWR mode							
8105E Series	LDO mode							

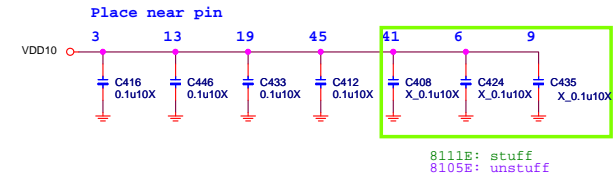
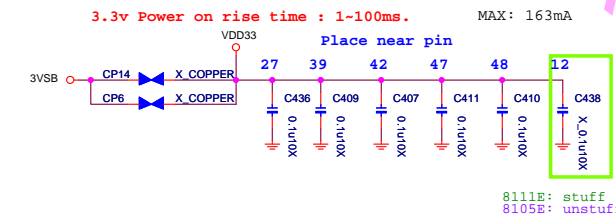
RTL8105E 10/100M LAN co-layer RTL8111E Giga LAN



For RTL8111E Series EEPROM / ASF / Efuse Function

	EEPROM 93C46	EEPROM 93C56/6	EEPROM 93C46	EFuse
SMBCLK	X	X	L	X
SMBDATA	L	H	H	L
GPO	H	H	H	H

Note: For RTL8111E-VL, R17 must be 1K.



8105E POWER Consumption

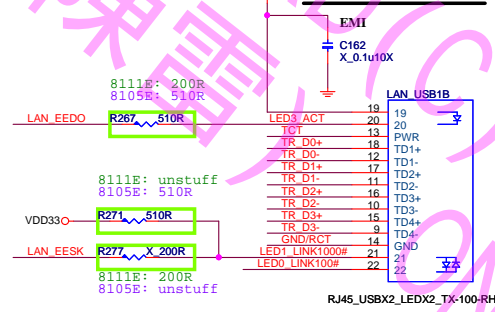
	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

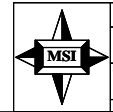
Pin49: 9 via from top layer to GND layer and make the via at the center of IC.

LAN Connector



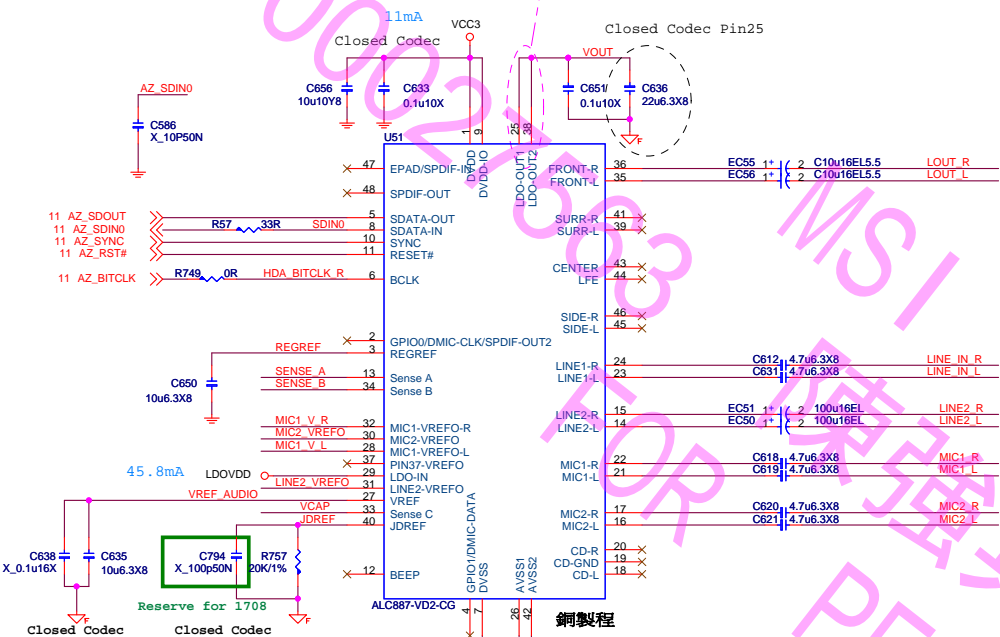
only support LED0+LED1+LED1+LED3 dual color LED combinations when using EEPROM

Giga-Lan		10/100-Lan	
N58-22F0731		N58-22F0731	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
20		20	
21		21	
22		22	

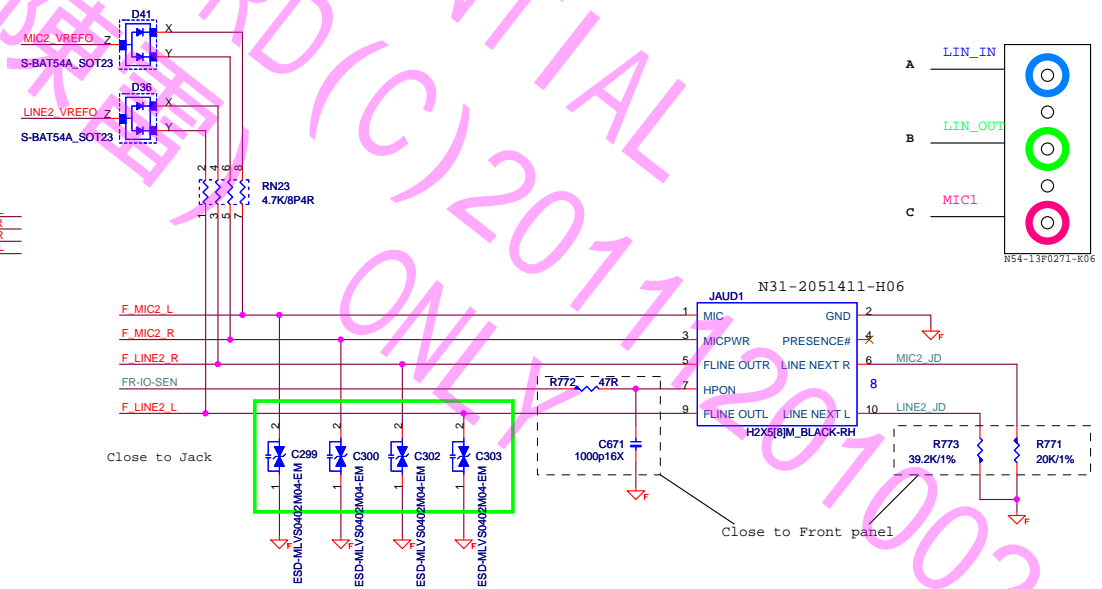
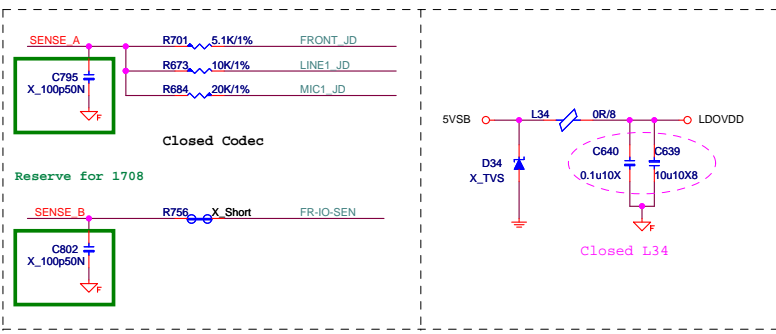
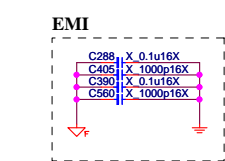
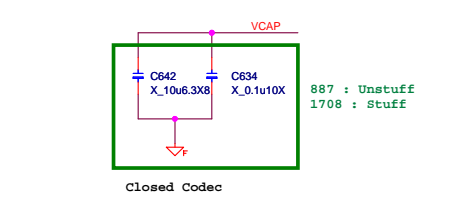
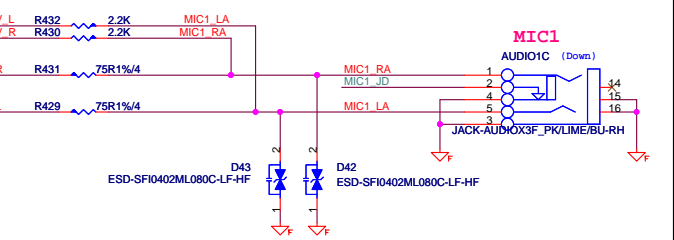
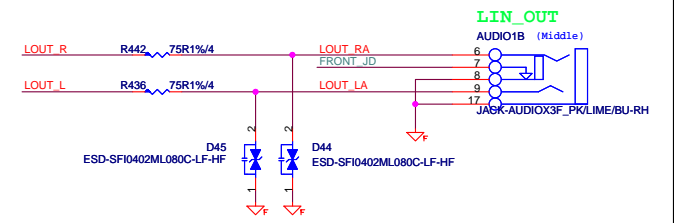
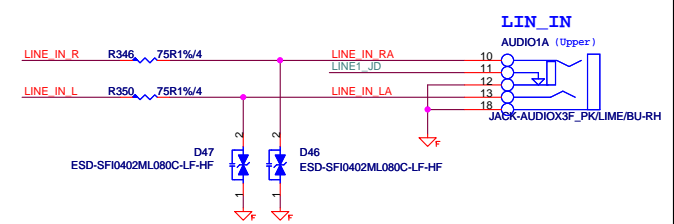
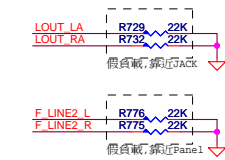


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Codec Pin25 & 38連接的Layout，以最短路徑，至少40mils線寬連接。



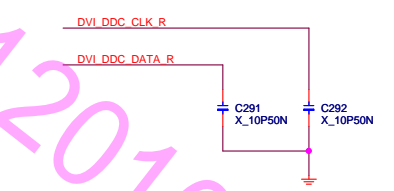
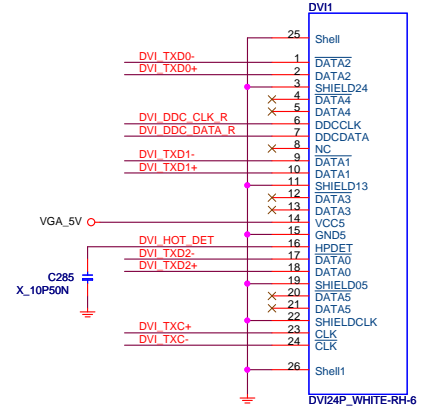
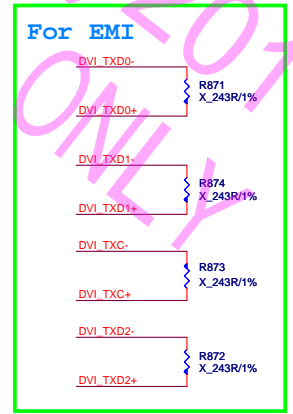
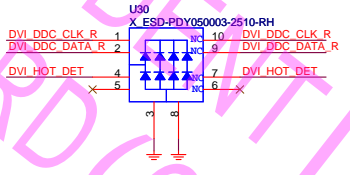
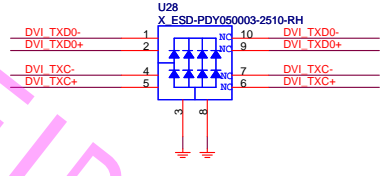
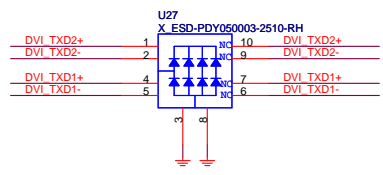
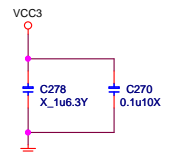
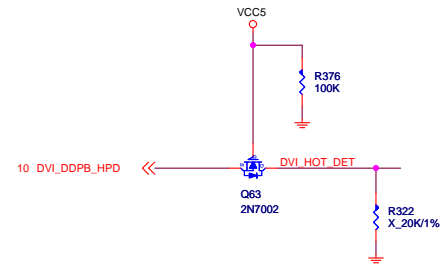
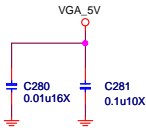
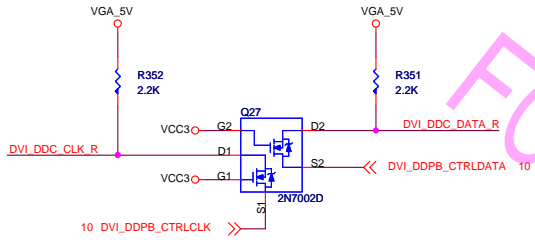
當串接電容有極性時，需上對地電阻



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DVI level shifter

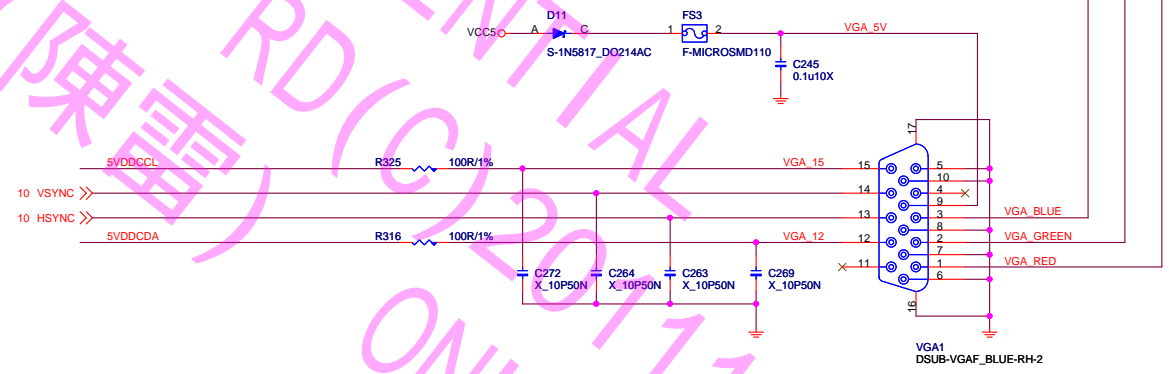
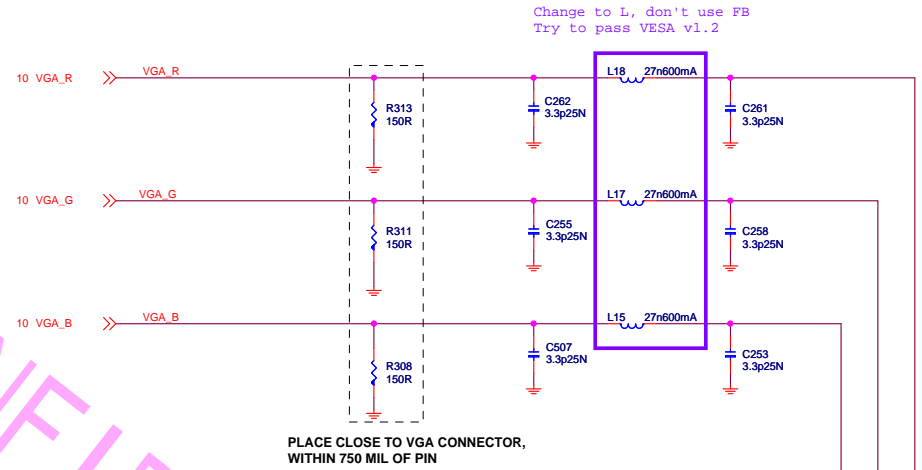
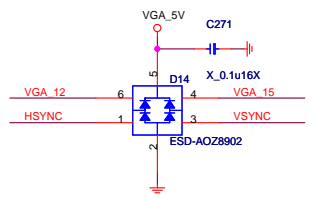
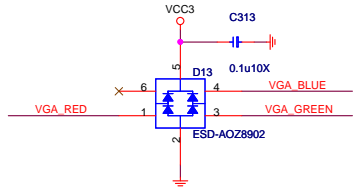
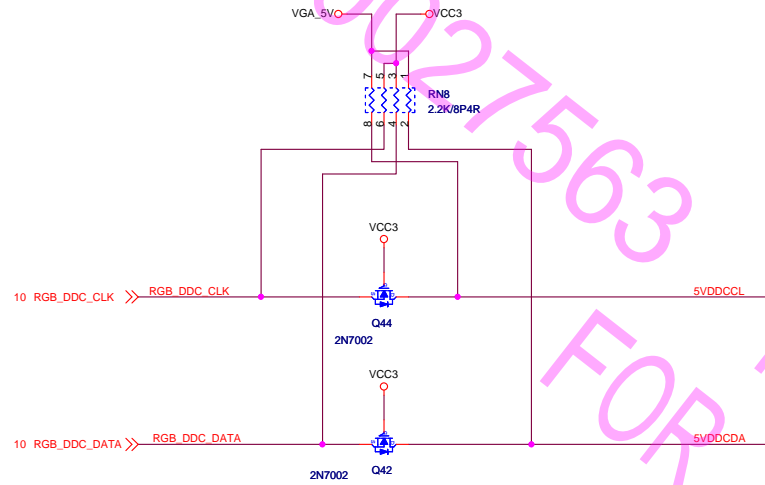
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift

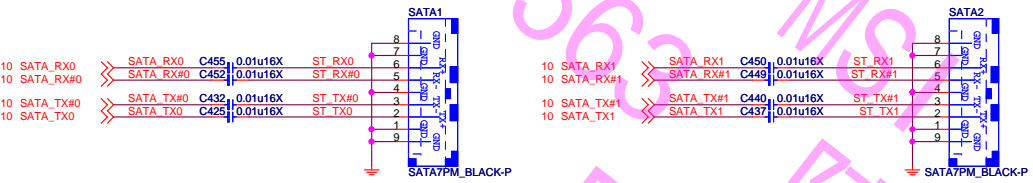


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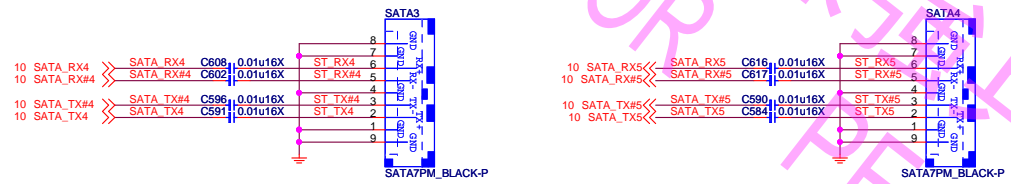
Table 1-3. Desktop Intel® 6 Series Chipset SKUs

Feature Set	SKU Name(s)					
	Q67	Q65	B65	H67	P67	H61
Total number of SATA ports	6	6	6	6	6	4
• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)	2 ⁴	1 ⁵	1 ⁵	2 ⁴	2 ⁴	0
• SATA Ports (3 Gb/s and 1.5 Gb/s only)	4	5	5	4	4	4 ⁸

NOTES:
8. SATA ports 2 and 3 are disabled.
SATA 3G PORT 0,1

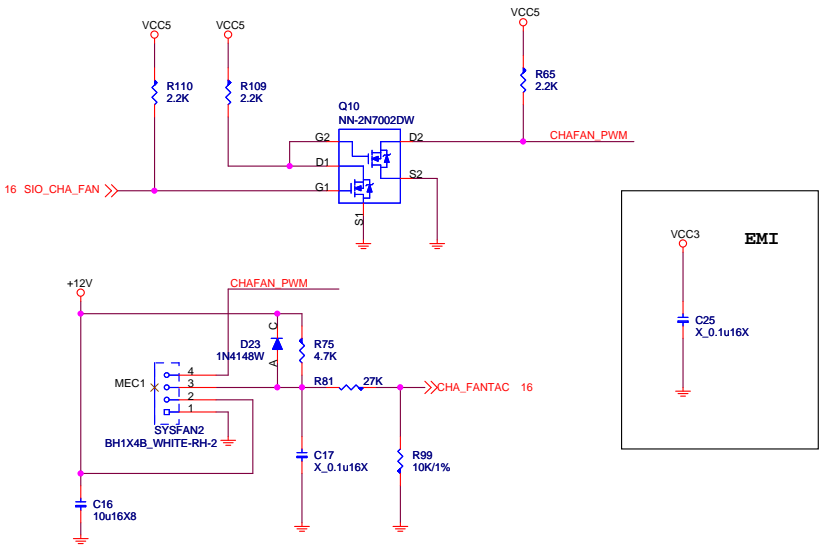


SATA 3G PORT 4,5



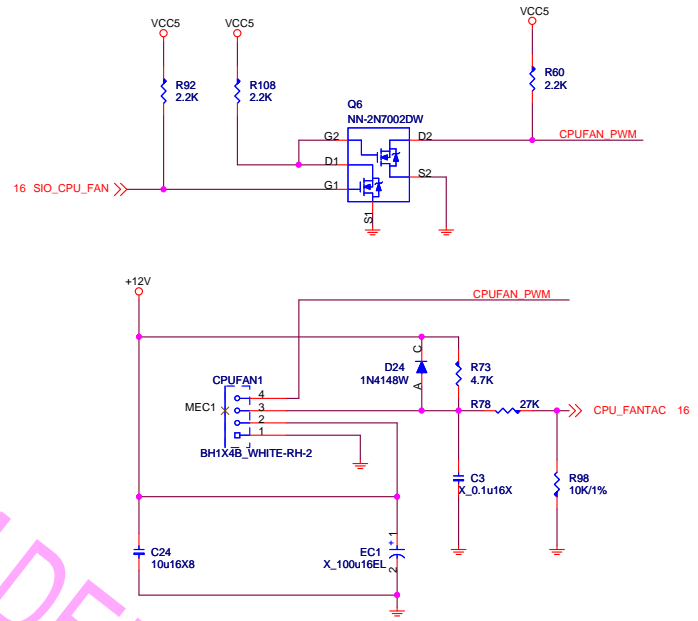
CHASSIS FAN-COUNTROL CIRCUIT

From SIO SYSTEM FAN2



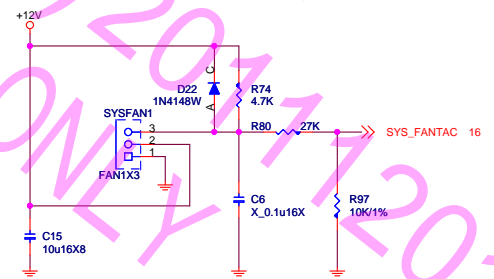
CPU FAN-COUNTROL CIRCUIT

From SIO SYSTEM FAN1



SYSTEM FAN3-COUNTROL CIRCUIT

From SIO SYSTEM FAN3



5V_USB Switch

5V_USB must 120mm



Default VCC5 (PIN1-3,2-4)

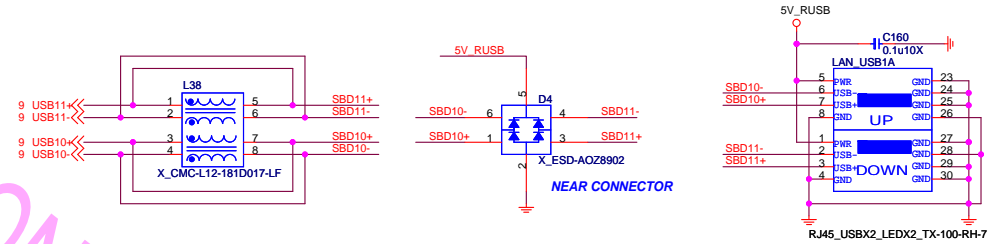
JUSB_PW1	BIOS Menu	Wake up support
1-3,2-4	EUP Enable	Not support
3-5,4-6	EUP Disable	Not support
3-5,4-6	EUP Enable	Not support
3-5,4-6	EUP Disable	support

Rear USB Connector

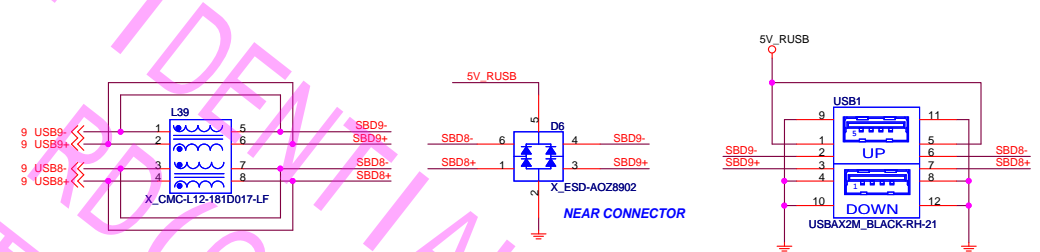
NEAR USB REAR CONNECTOR



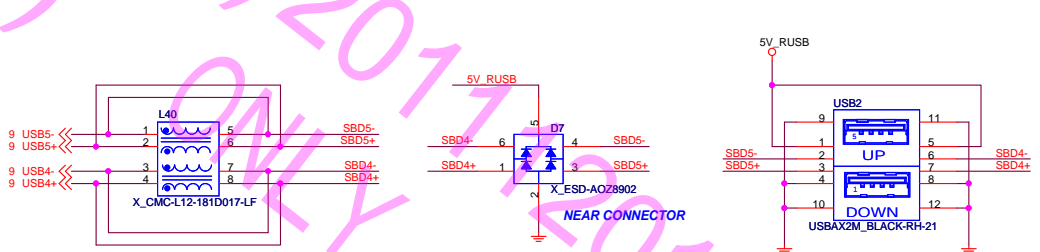
REAR USB PORT 10,11 (With LAN)



REAR USB PORT 8,9



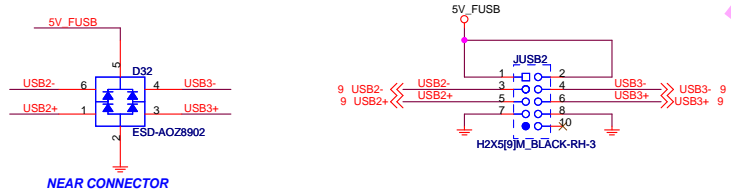
REAL USB PORT 4,5



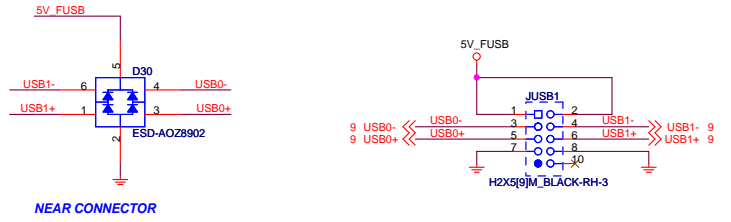
Front USB Connector

For H61 6,7,12,13 Port should be remove

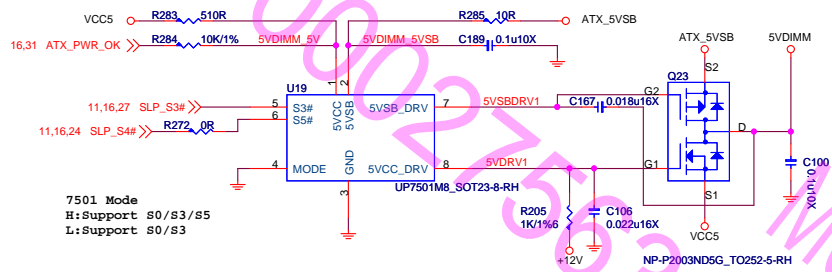
FRONT USB PORT 2,3



FRONT USB PORT 0,1

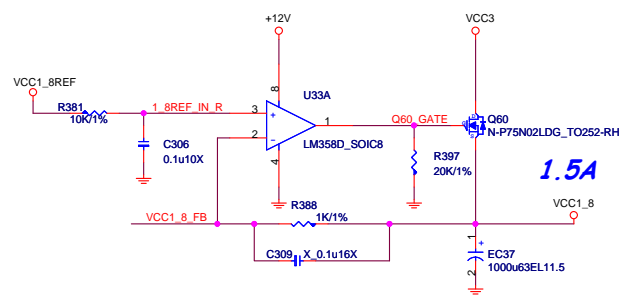
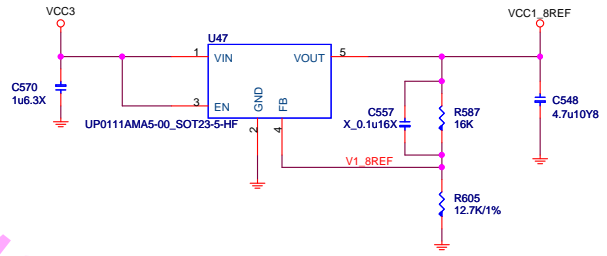


5VDIMM FOR DDR

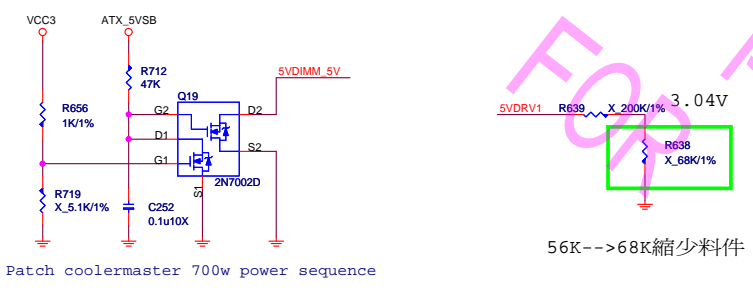


7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

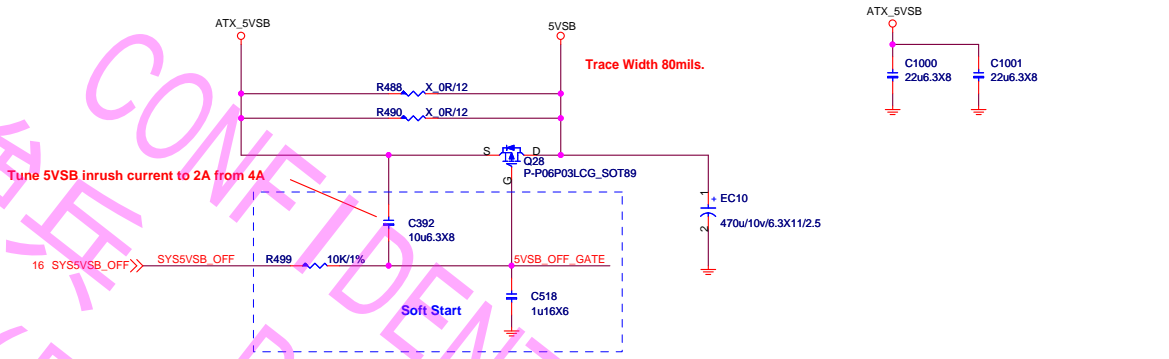
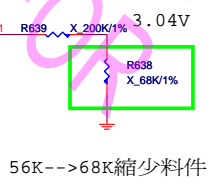
VCC1_8REF



5VSB Power Switch



Patch coolermaster 700w power sequence

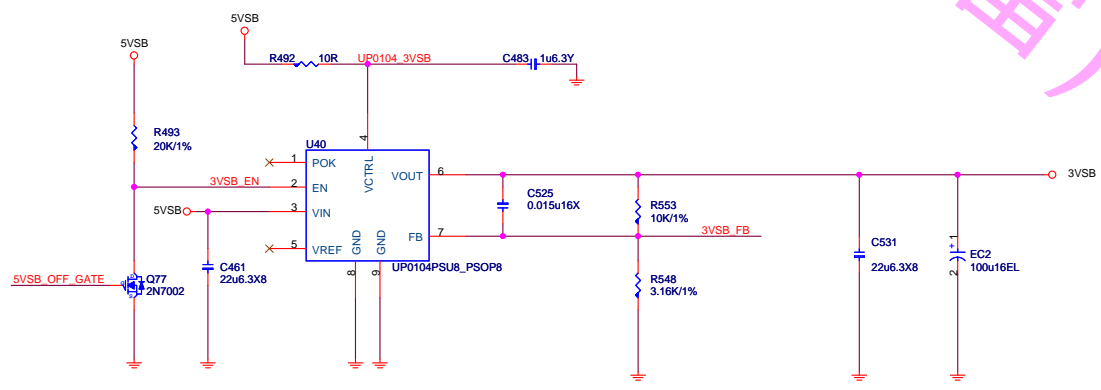


Tune 5VSB inrush current to 2A from 4A

Soft Start

3VSB

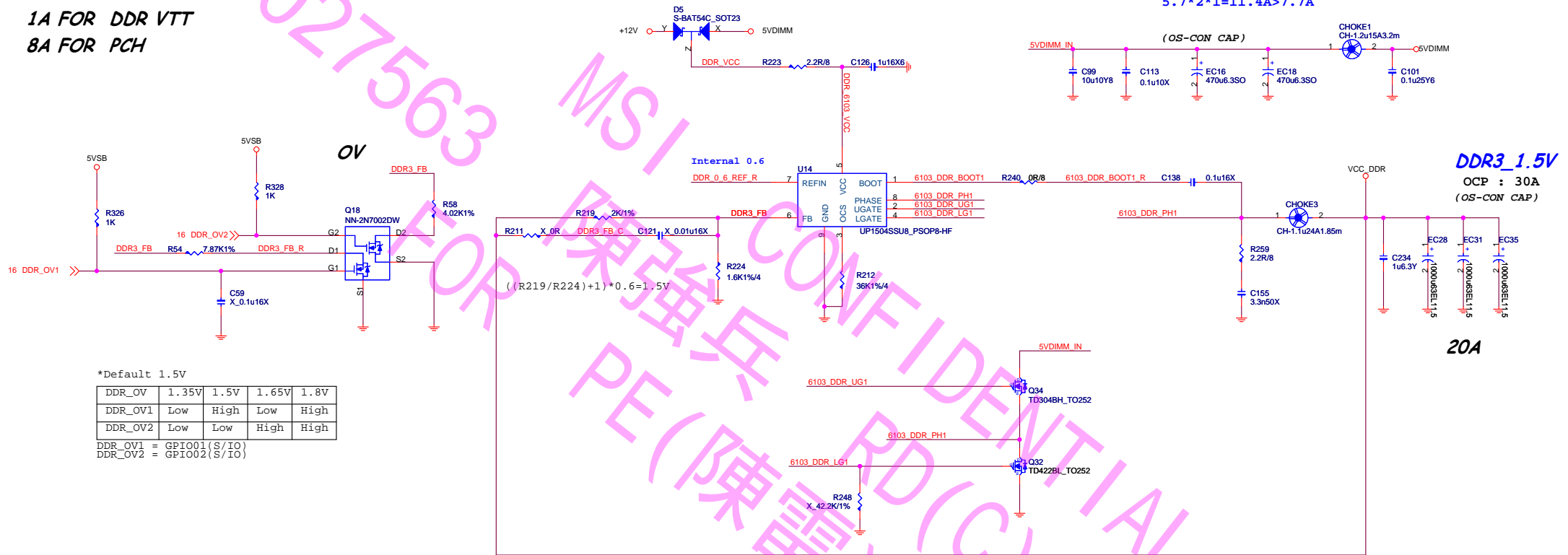
3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



DDR3_1.5V 4.5A+6A+1A+8A=19.5A

4.5A FOR CPU
6A FOR 2DIMM
1A FOR DDR VTT
8A FOR PCH

Ripple=7.7A
 $5.7*2*1=11.4A > 7.7A$

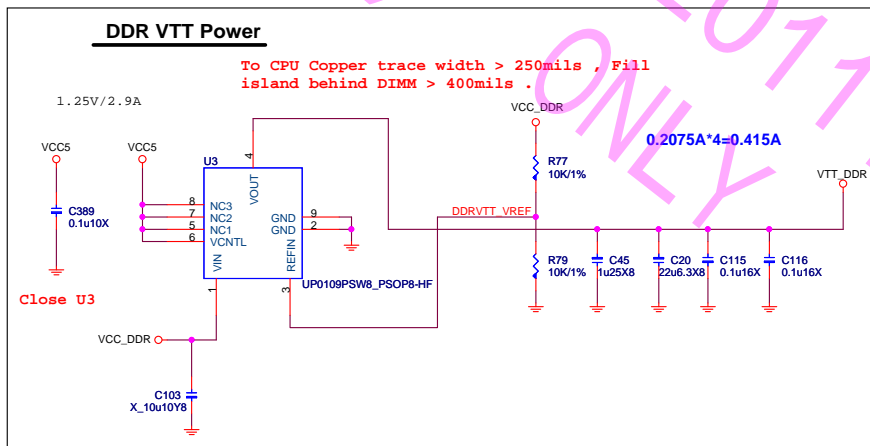
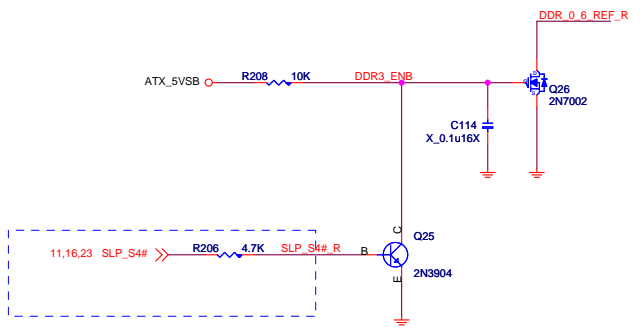


*Default 1.5V

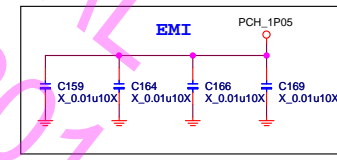
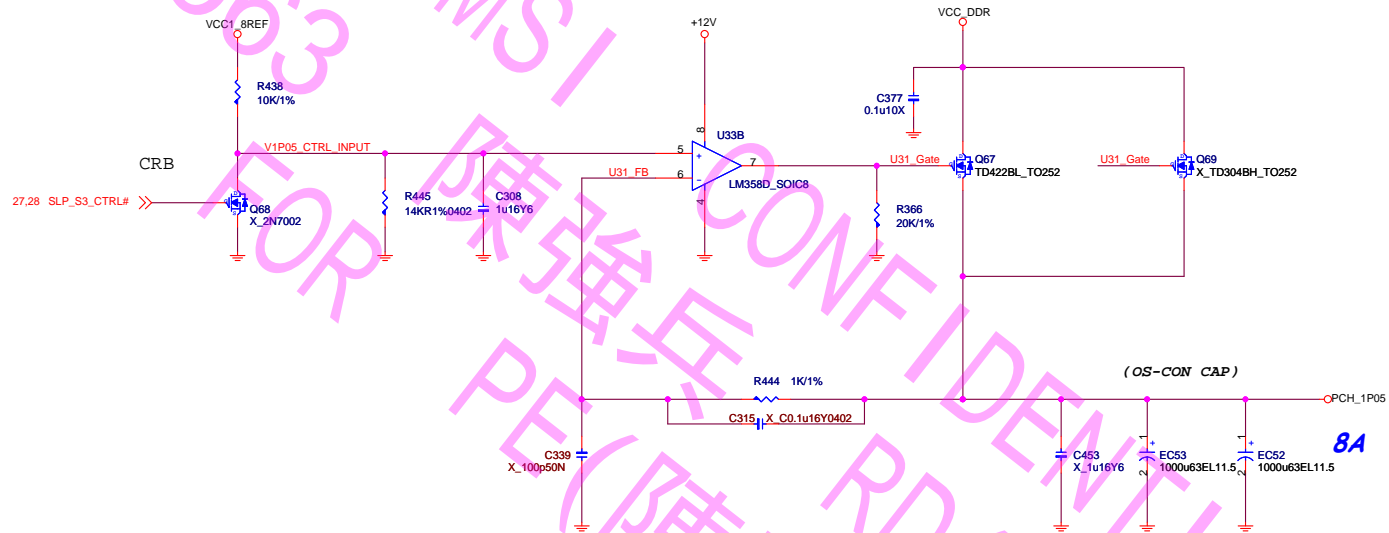
DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR_OV1 = GPIO01(S/IO)
DDR_OV2 = GPIO02(S/IO)

P.S. Only for meet Intel power down sequence.



PCH Power:1.05V

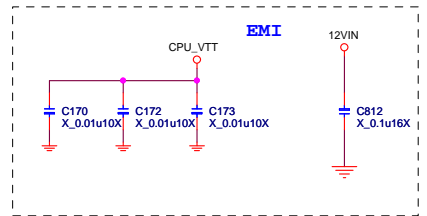
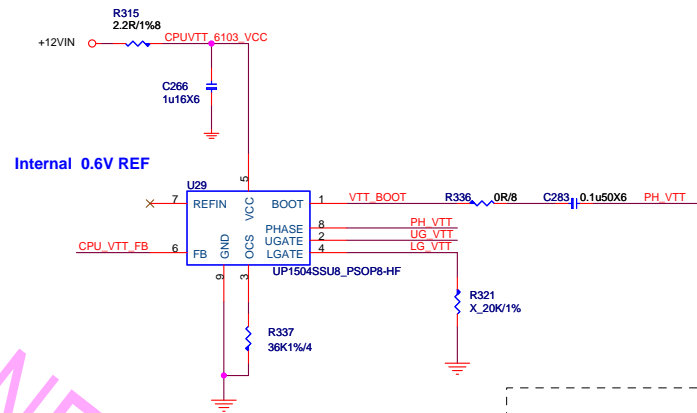
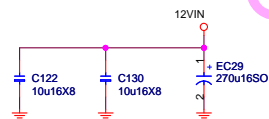


MICRO-STAR INT'L CO.,LTD		
MS-7788		
Size Custom	Document Description PCH Power - OP+MOS	Rev 10
Date: Thursday, November 24, 2011	Sheet 25 of	33

CPU_VTT:1.05/1.00

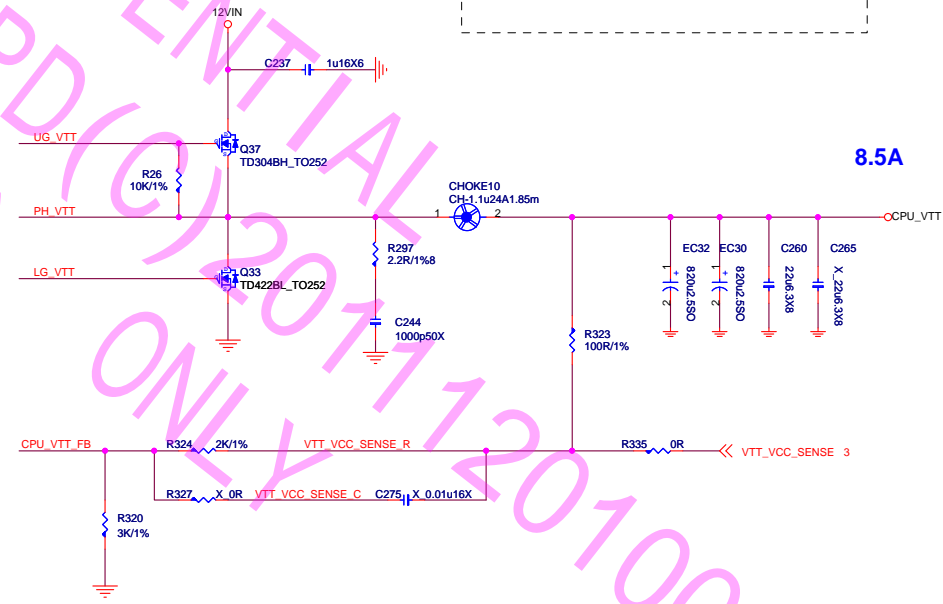
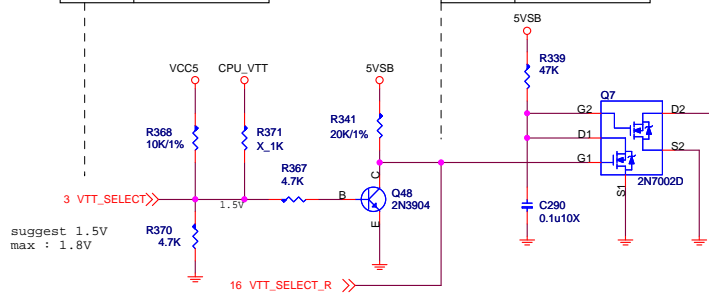
$CPU\ VTT\ 8.5A + SA\ Core = 8.8A = 17.3A$

$I_{ripple} = 1.92(vtt) + 1.88(sa)$
 $5 * 1 = 5A > 3.8A$



VTT_SELECT	
Low	1.0V
High	1.05V

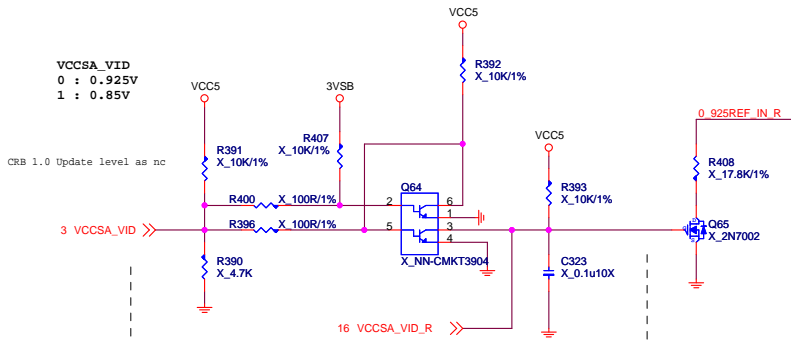
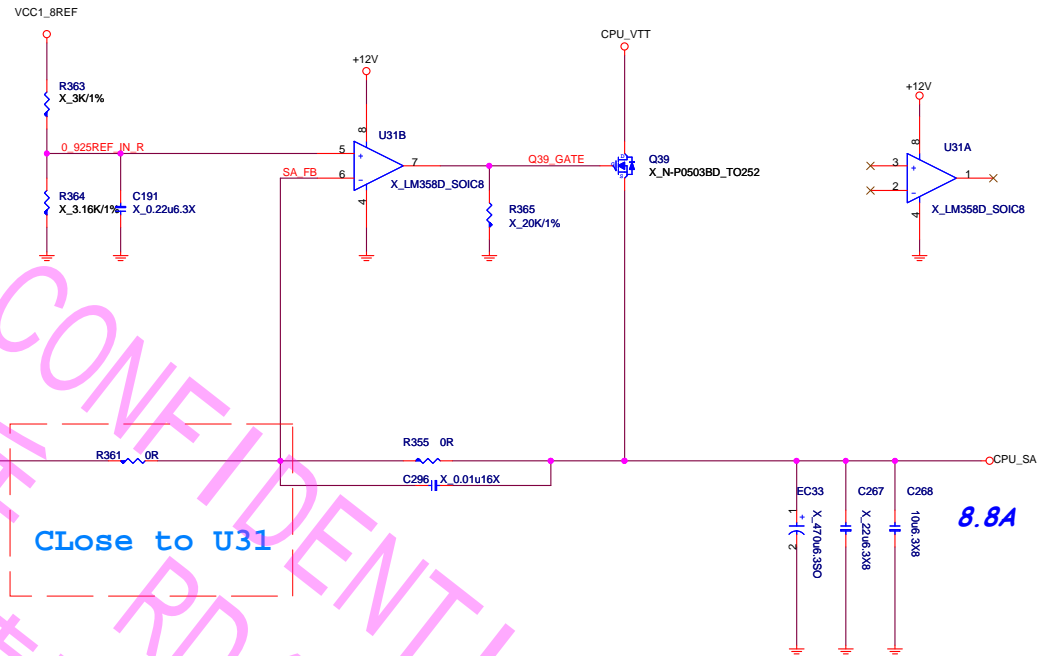
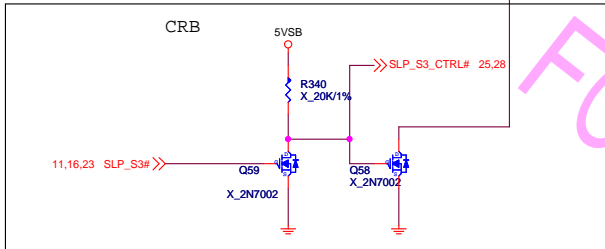
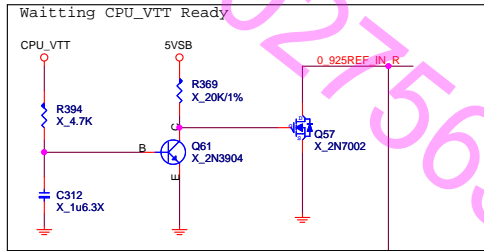
VTT_SELECT Table	
Low	1.05V
High	1.0V



MICRO-STAR INT'L CO.,LTD		
MS-7788		
Size Custom	Document Description CPU_VTT - UP1504 1-Phase	Rev 10
Date: Thursday, November 24, 2011	Sheet 26	of 33

CPU_SA:0.925/0.85

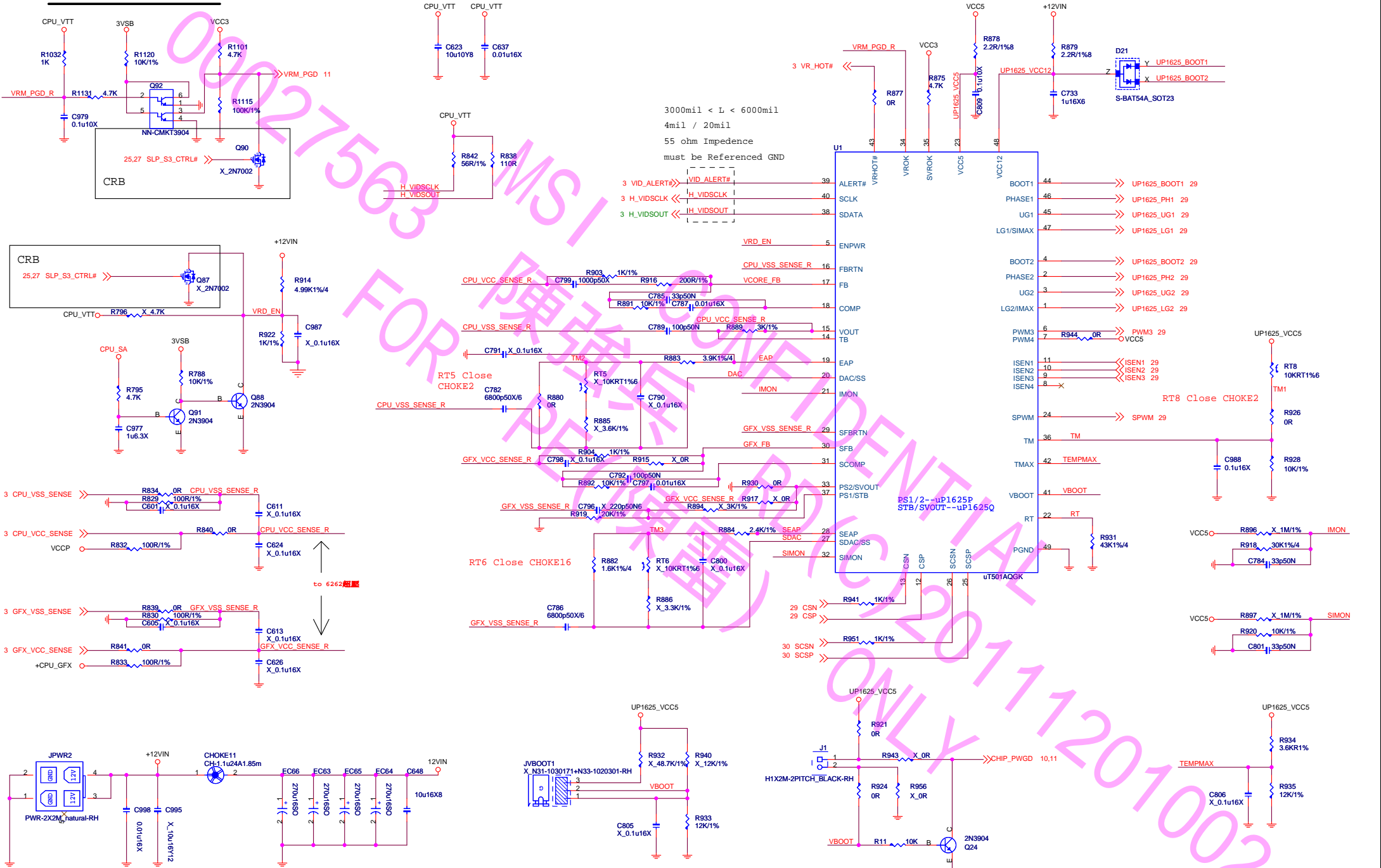
SA Core = 8.8A



VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V

VRMPWRGD LEVEL SHIFT



3000mil < L < 6000mil
4mil / 20mil
55 ohm Impedence
must be Referenced GND

3 VID_ALERT#>>VID_ALERT#>
3 H_VIDSCLK<<H_VIDSCLK<<
3 H_VIDSOUT<<H_VIDSOUT<<

RT5 Close
CHOKE2

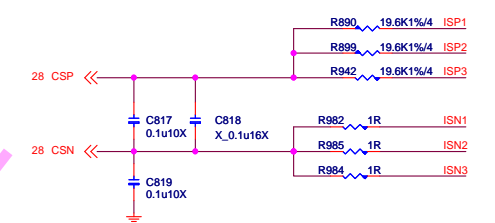
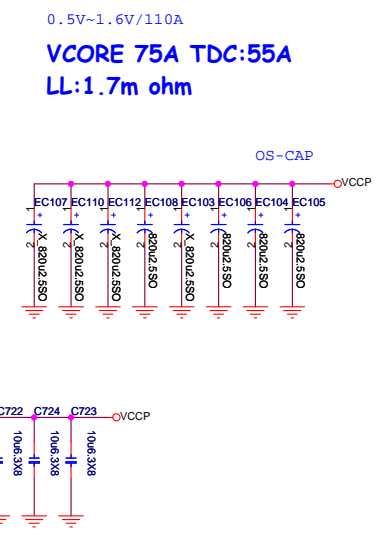
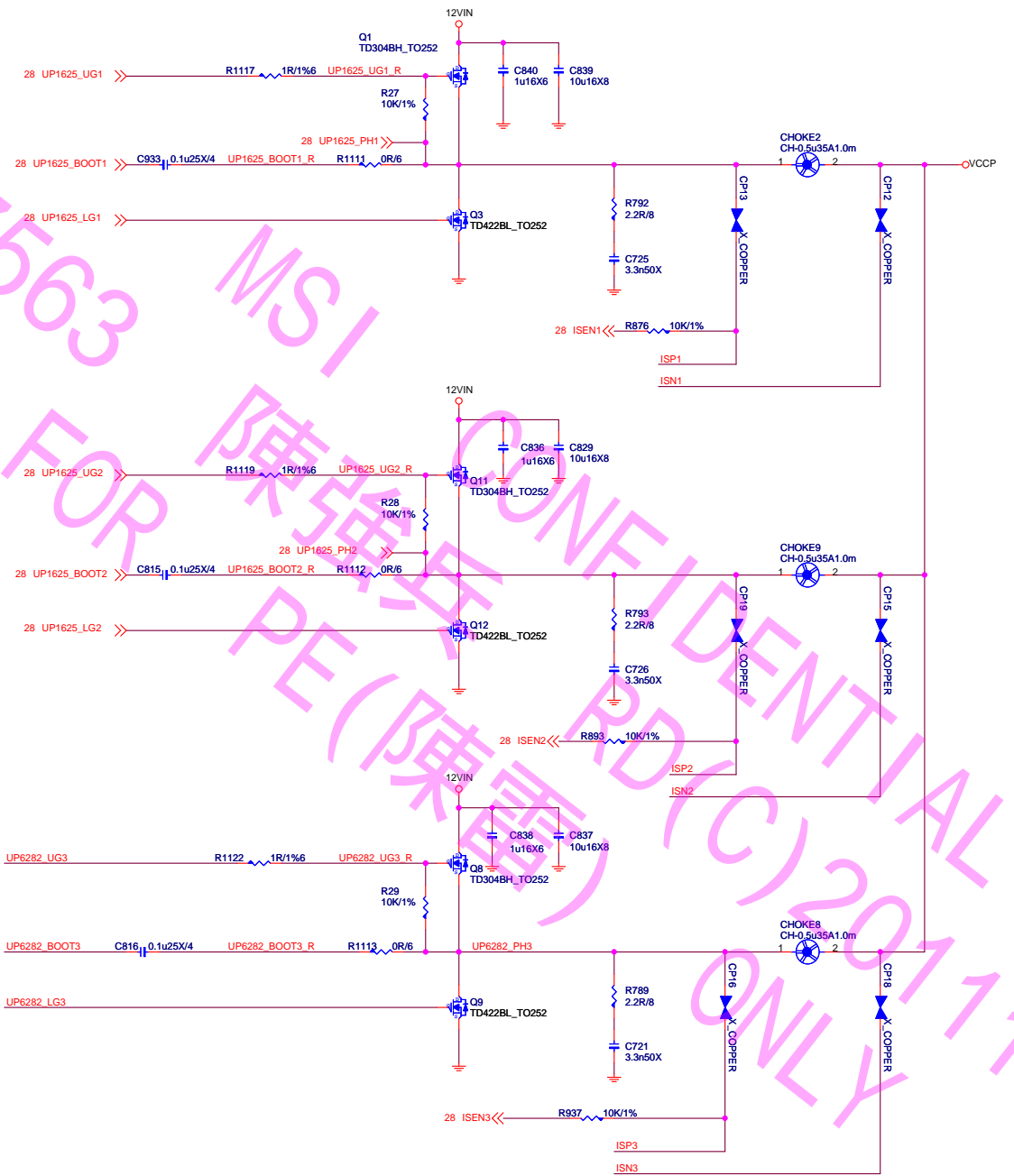
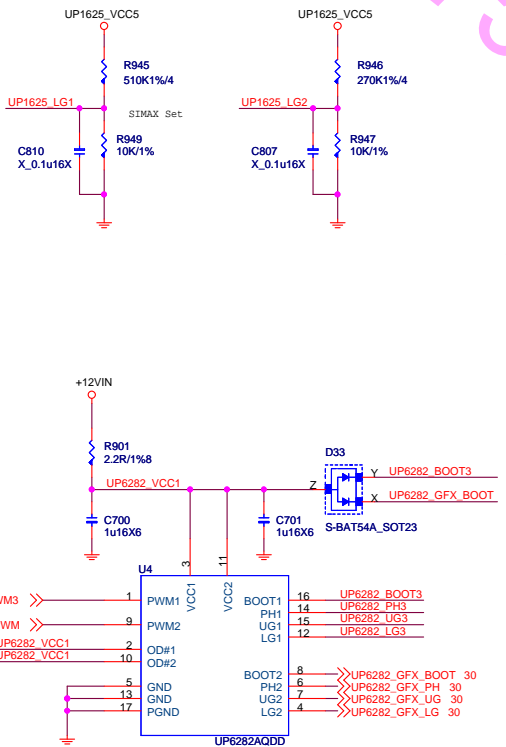
RT6 Close
CHOKE16

RT8 Close
CHOKE2

Use PWM IC I32-UT5010C-U33(old) --> stuff JVboot1/R932/R933/J1/R943/R956
Use PWM IC I32-UT5011C-U33(new) --> stuff J1/R933/R921/R924/R11/Q24

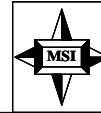
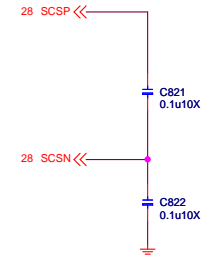
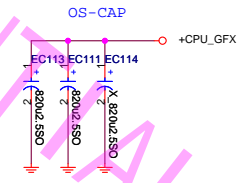
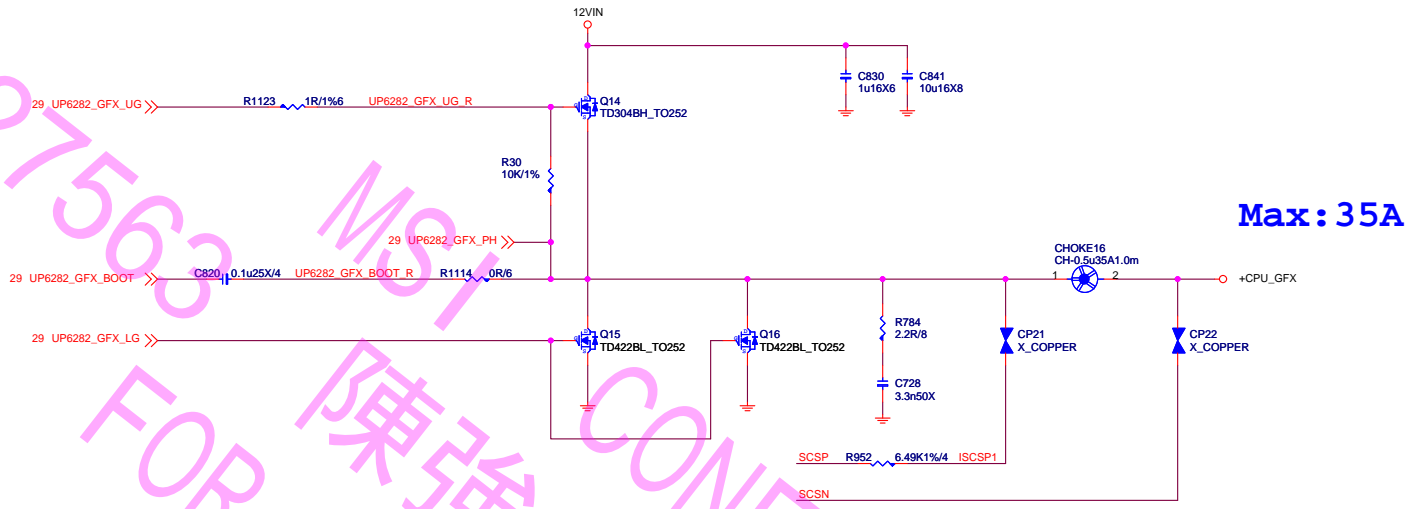
		MICRO-STAR INT'L CO.,LTD	
		MS-7788	
Size Custom	Document Description VRD12 - UT501 3+1-Phase		Rev 10
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00027563 MSI FOR 陳學軍 (陳學軍) ONLY 20111201002



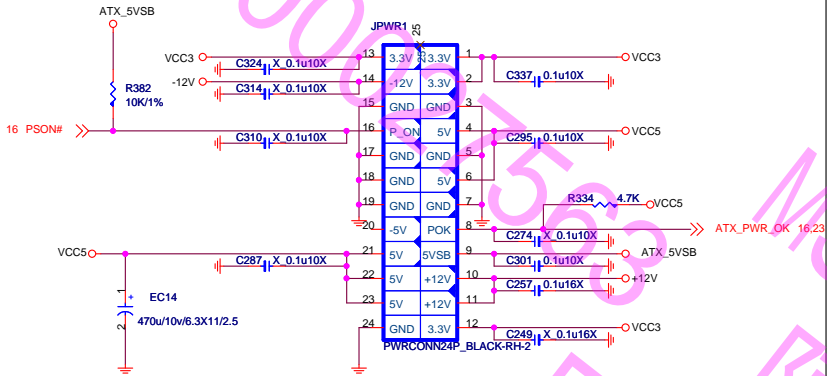
0.5V~1.6V/110A
VCORE 75A TDC:55A
LL:1.7m ohm

00027563
MSI
FOR 陳強兵 CONFIDENTIAL RD(C)20111201002
PE (陳雷)
ONLY



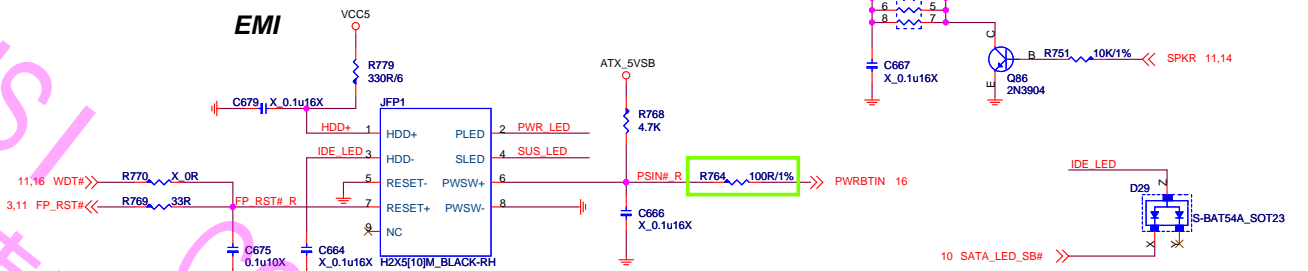
MICRO-STAR INT'L CO.,LTD		
MS-7788		
Size Custom	Document Description UP6234 1-Phase GPU	Rev 10
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ATX POWER CONNECTOR

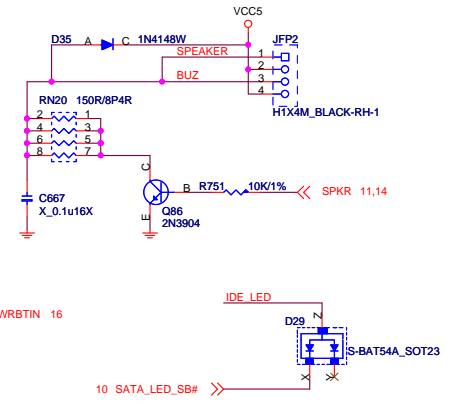


FRONT PANEL

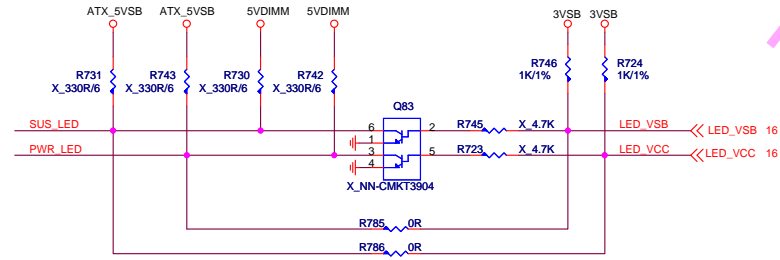
EMI



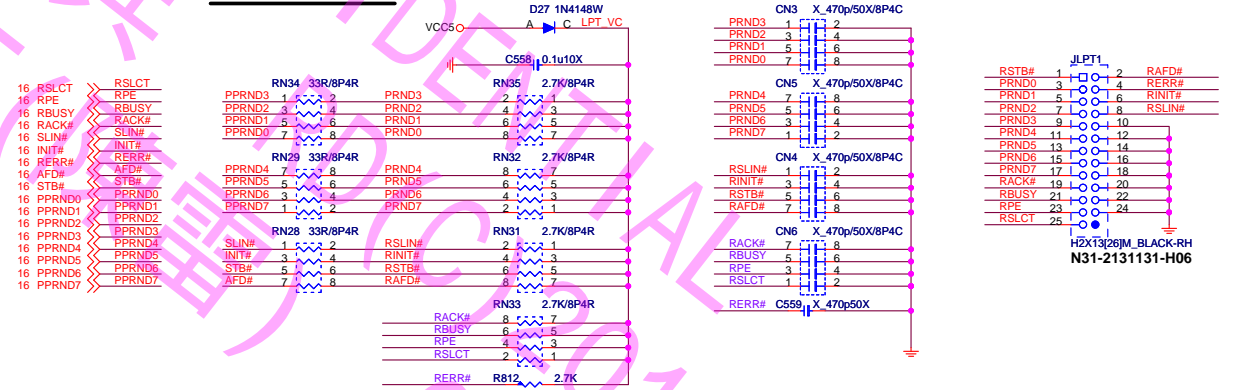
Speaker Pin Header



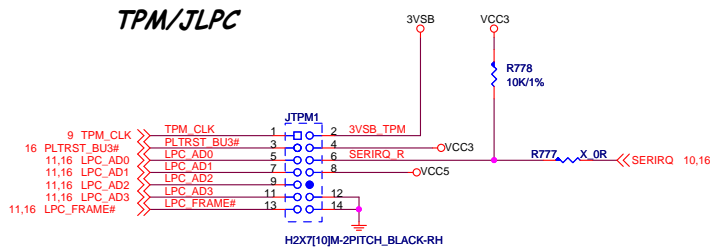
LED (for Fintek 71868)



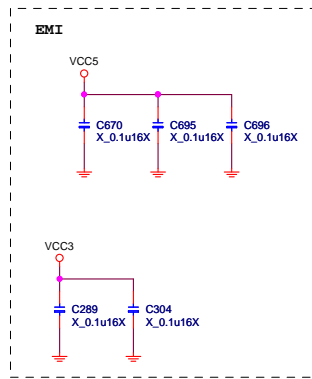
PARALLAL PORT



TPM/JLPC



EMI



MICRO-STAR INT'L CO.,LTD

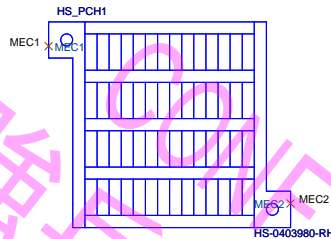
MS-7788

Size	Document Description	Rev
Custom	ATX PWR-Connector & Front Panel & EMI	10
Date:	Thursday, November 24, 2011	Sheet 31 of 33

MS-7680-5.1

OPT	Configure	BOM	Function
A	H61M-P30 (B3)	601-7680-300	H61M-P30 (B3), H61 B3, 2*DDRIII, 1*PCI-Ex16, 2*PCI-Ex1, Gb Lan, 4*SATAII, 10*USB2.0, HD 8Ch Audio, DVI/D-sub, All Solid Cap, EuP, RoHS
B	H61M-P20 (B3)	601-7680-20S	H61M-P22 (B3), H61 B3, 2*DDRIII, 1*PCI-Ex16, 2*PCI-Ex1, 10/100 Lan, 4*SATAII, 10*USB2.0, HD 8Ch Audio(3 hole), DVI/D-sub, Half Solid Cap, EuP, RoHS
C	H61M-P25 (B3)	601-7680-310	H61M-P25 (B3), H61 B3, 2*DDRIII, 1*PCI-Ex16, 2*PCI-Ex1, Gb Lan, 4*SATAII, 10*USB2.0, HD 8Ch Audio(3 hole), DVI/D-sub, Half Solid Cap, EuP, RoHS
D	H61M-P22 (B3)	601-7680-320	H61M-P22 (B3), H61 B3, 2*DDRIII, 1*PCI-Ex16, 2*PCI-Ex1, 10/100 Lan, 4*SATAII, 10*USB2.0, HD 8Ch Audio(3 hole), DVI/D-sub, Half Solid Cap, EuP, RoHS

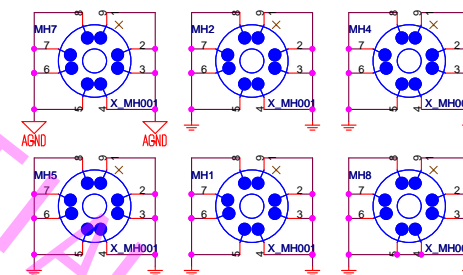
PCH XDP PWRGD/RESET



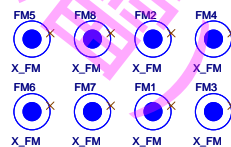
Simulation



Mounting Holes



Optical Fiducial Marks-120



7788-10

PK0-0768051-E36, E&E, 23, 寶安恩斯邁廠 (MSIS), 4, Coffee
 PK0-0768051-E36, E&E, 27, 寶安恩斯邁廠 (MSIS), 4, Coffee
 PK0-0768051-G37, 精成, 23, 寶安恩斯邁廠 (MSIS), 4, Coffee
 PK0-0768051-G37, 精成, 27, 寶安恩斯邁廠 (MSIS), 4, Coffee



BAT-BCR2032P-RH



X_Rubber



X_Rubber



E21-7557050-L06

	MICRO-STAR INT'L CO.,LTD	
	MS-7788	
	Size Custom	Document Description XDP / Manual Parts
Date: Thursday, November 24, 2011		Sheet 32 of 33

MS-7680 5.1 Change to MS-7778 0A

1. 7.1-Channel Audio out change to 5.1-Channel Audio out.
2. Remove PCIe X1 slot (PCI_E3).
3. Remove SPIDF out.
4. Remove Front USB port*2 (JUSB3).
5. JLPT1 2mm pitch change to 2.54mm pitch.

MS-7788 0A Change to MS-7788 1.0

1. modify VT501 COMP & SCOMP not connection to GND.
2. Vcore : E110 、EC112 、EC103 、EC107 >> N.C
C196 、C198 、C209 、C210 、C211 >> N.C
Vtt : C213 、C214 、C227 、C228 、C265 >> N.C
Vgfx : C109 、C203 、EC114 >> N.C
PWM : C782 、C786 Chang to 6.8nF ; R928 Change to 10K1%
By Power Solution.
3. Add C634 、C642 、C794 、C795 、C802 Empty By Audio codec ALC887 co-lay VT1708S CE.
4. Add C25 Empty By EMI Solution.
5. EC55 & EC56 DIP Footprint Change to SMD DIP Footprint (MSI P/N:C96-1001630-N07) By PM Request.