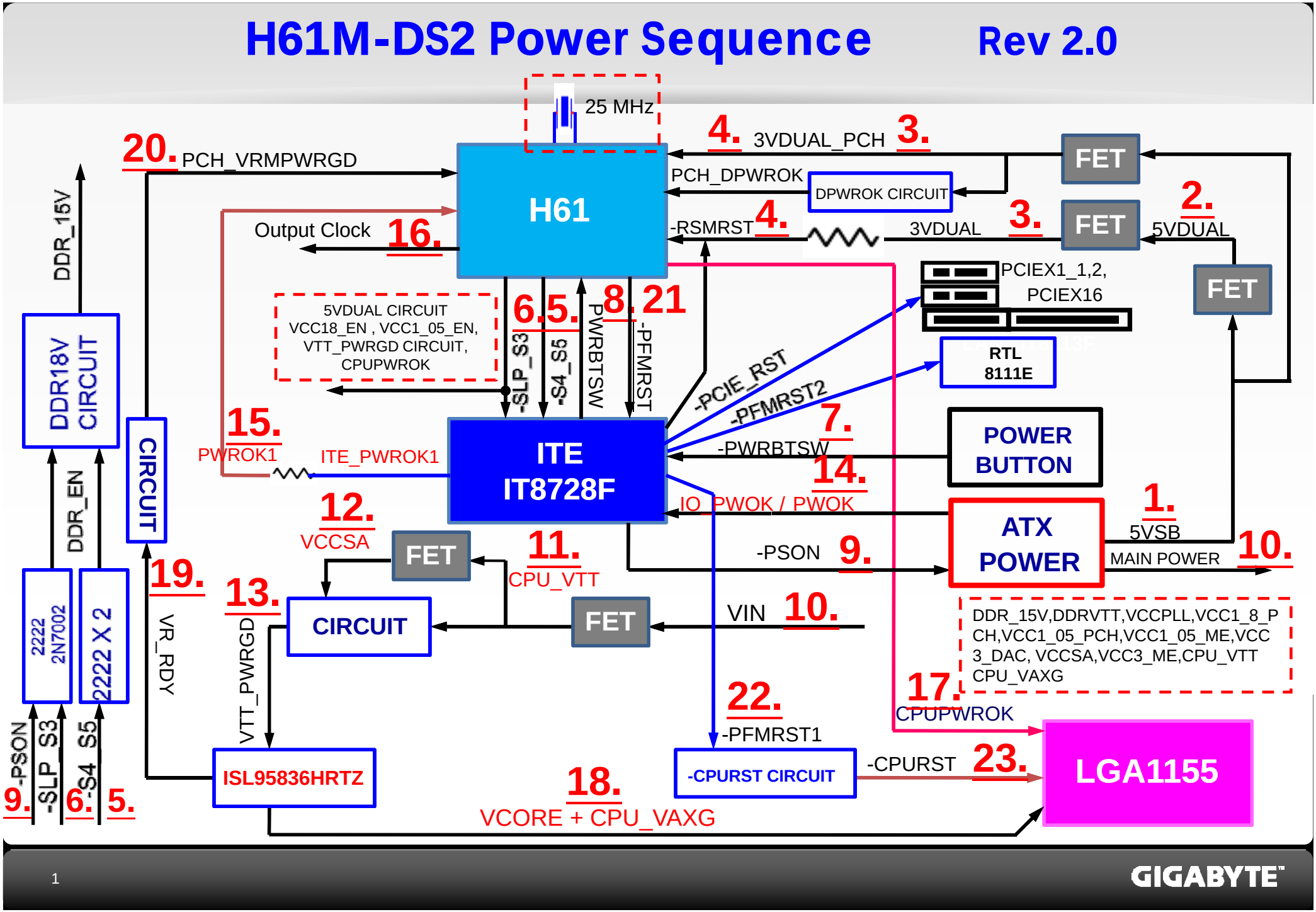
GIGABYTE™

H61M-DS2 Rev 2.0
Power Sequence & Power list

JEFF.KO

Since 1986

H61M-DS2 Power Sequence Rev 2.0



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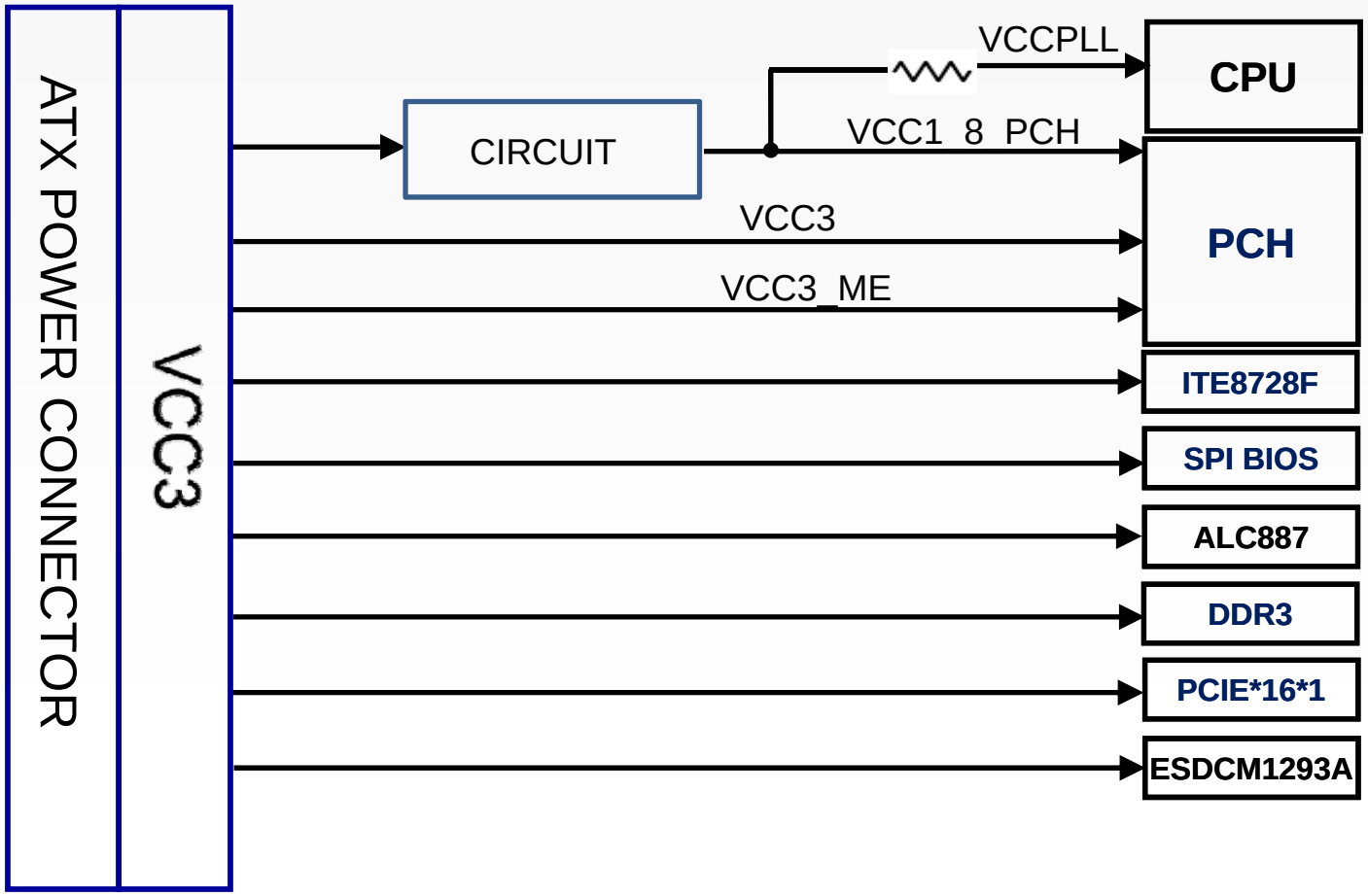
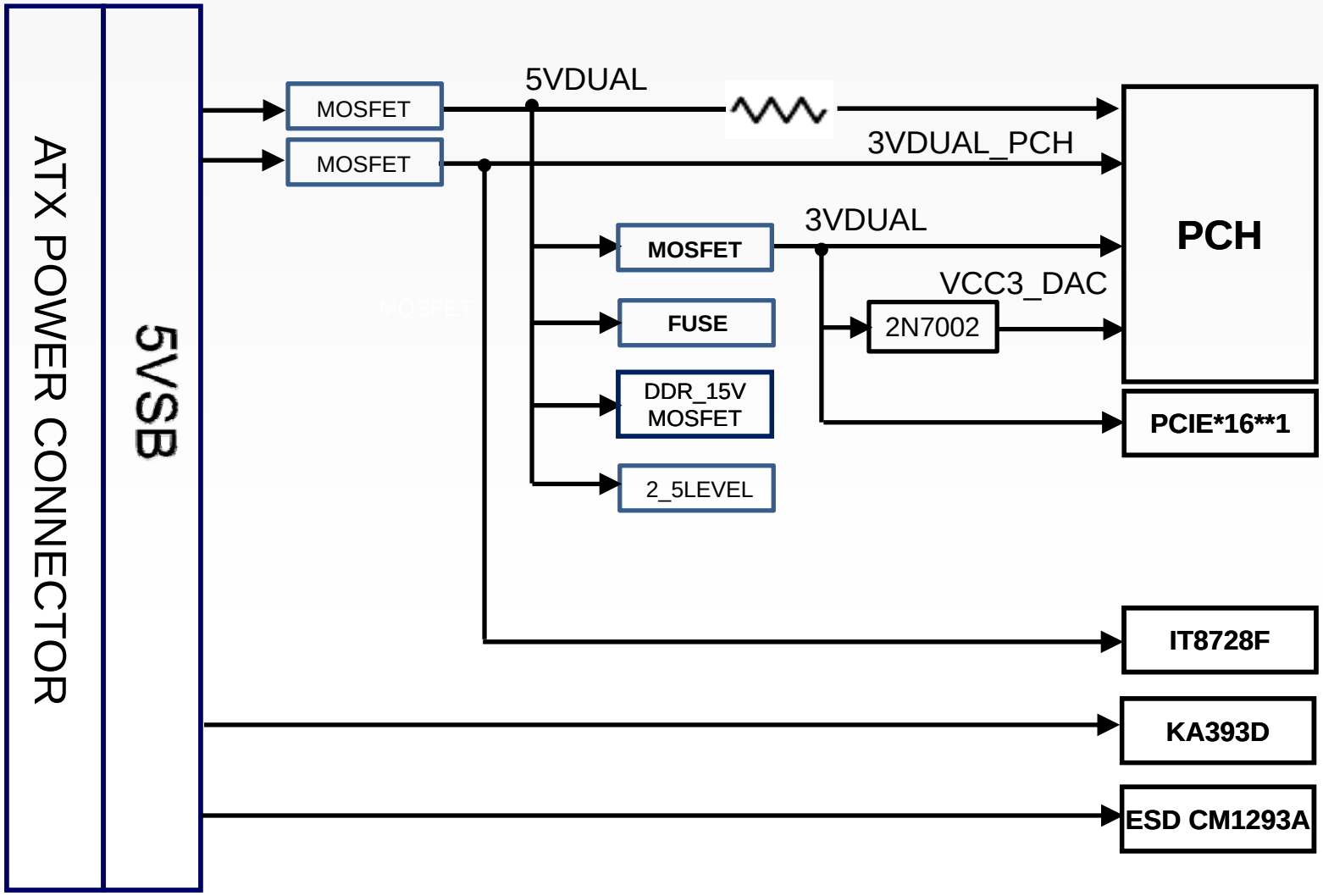
H61M-DS2 System Power / VCC3

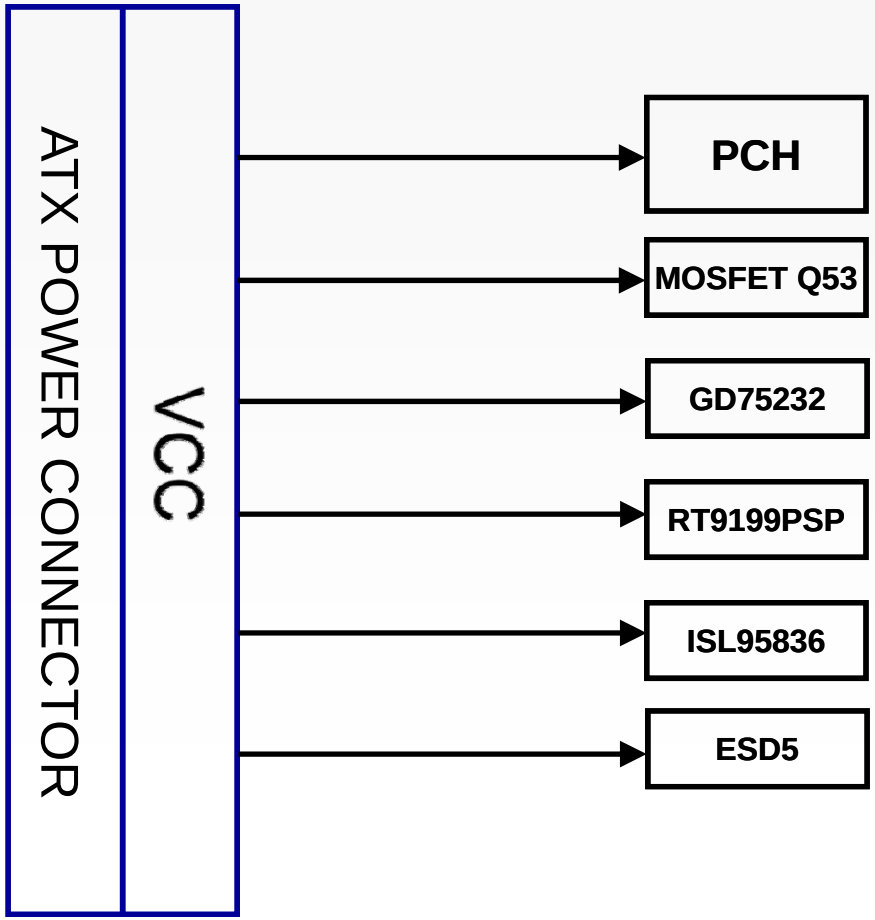
Rev 2.0



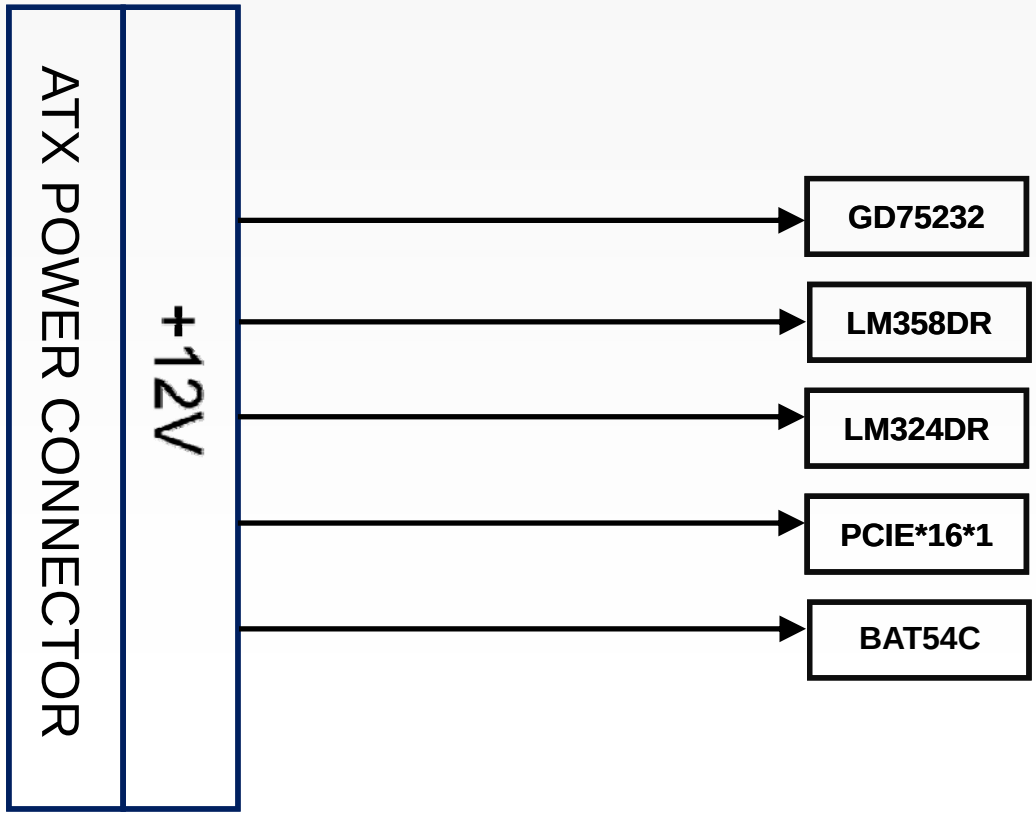
H61M-DS2 System Power / 5VSB Rev 2.0



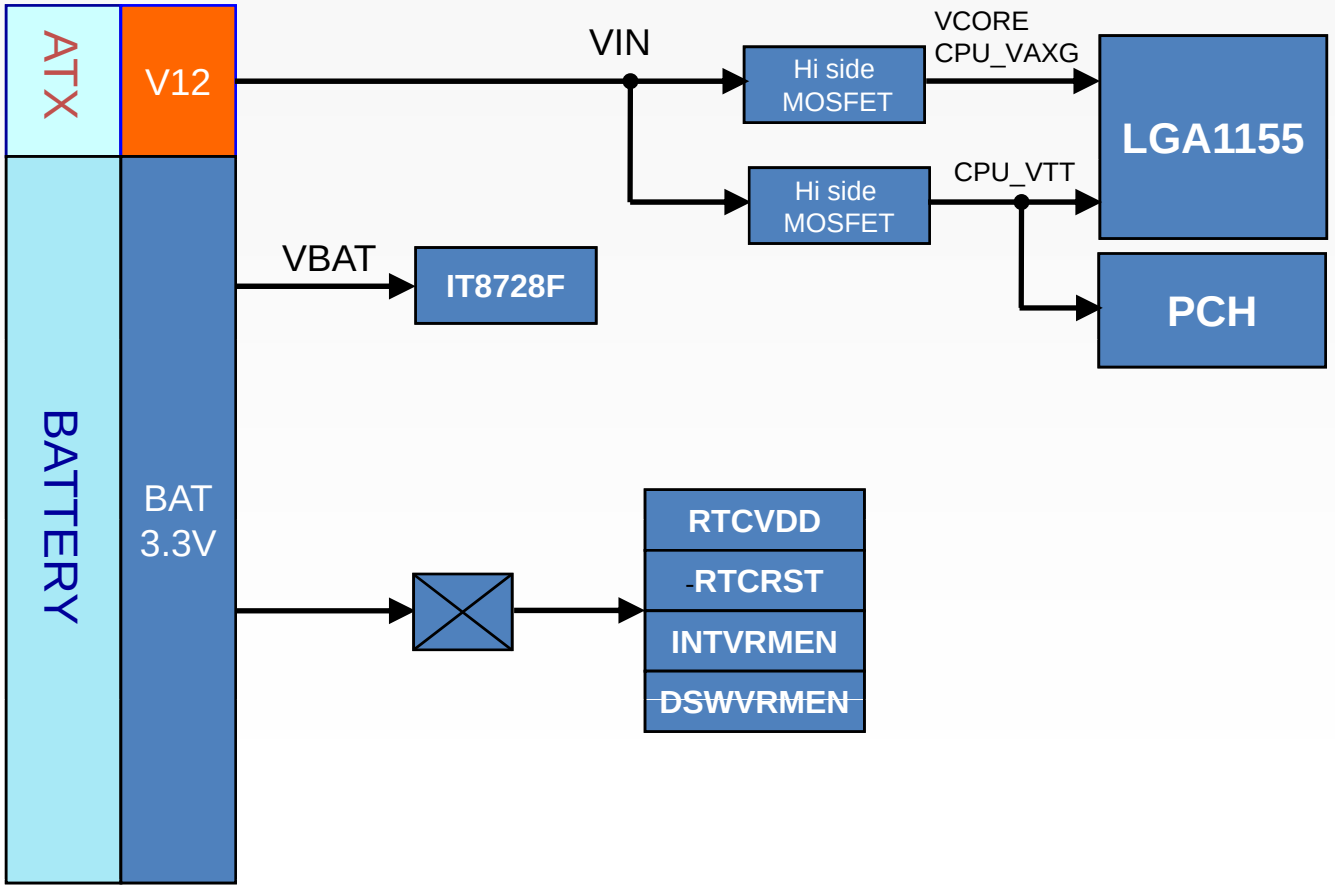
H61M-DS2 System Power / VCC Rev 2.0



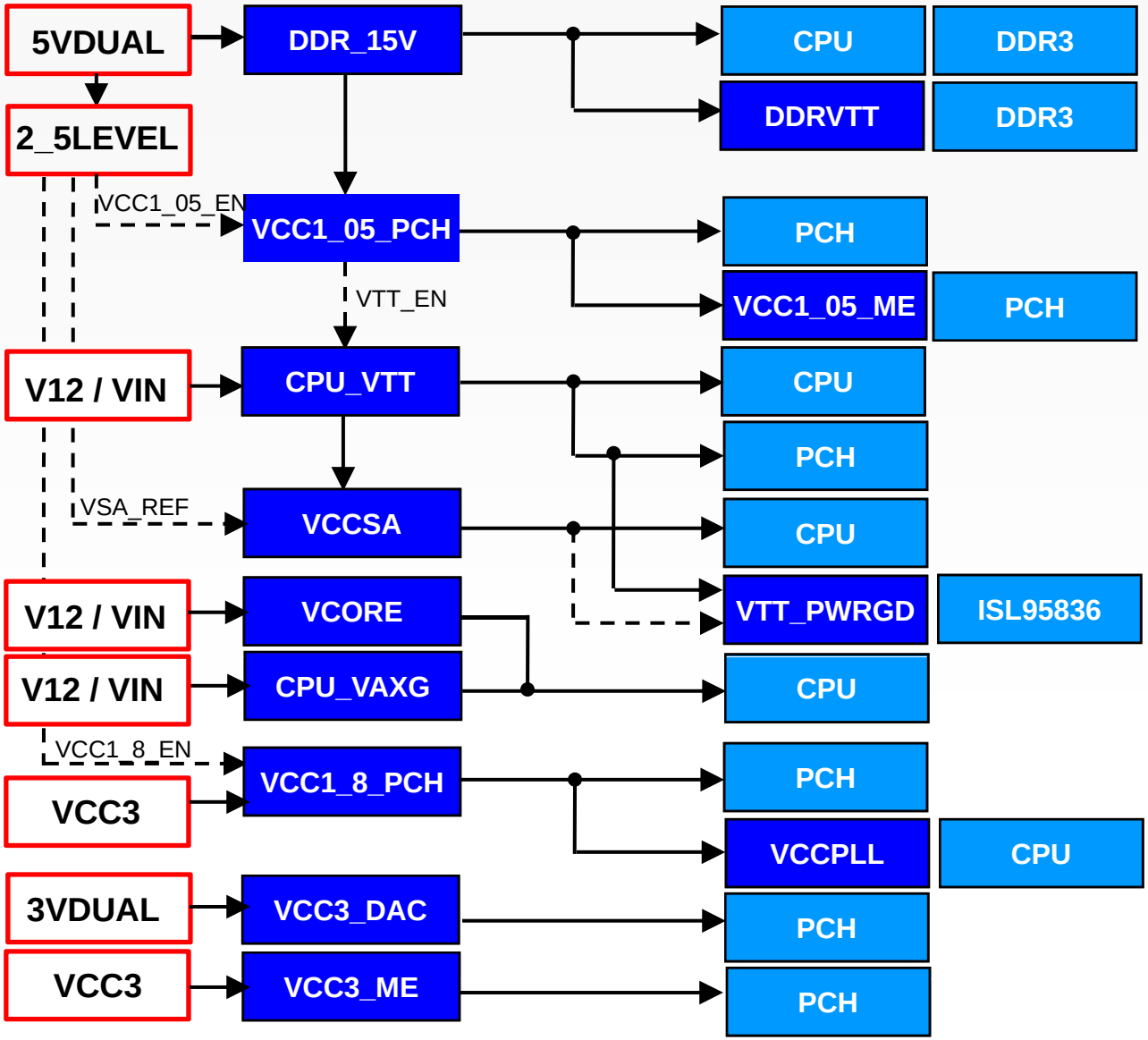
H61M-DS2 System Power / +12V Rev 2.0



H61M-DS2 System Power / V12 , BAT3.3V Rev 2.0



H61M-DS2 System Power Rev 2.0



CPU :
VCORE
CPU_VAXG
CPU_VTT
VCCSA
VCCPLL
DDR_15V

PCH :
VCC1_05_PCH
CPU_VTT
VCC1_8_PCH
VCC3_DAC
VCC3_ME
VCC1_05_ME

Power and Ground Signals

Name	Power	Description
DcpRTC	CAP pull low	Decoupling: This signal is for RTC decoupling only. This signal requires decoupling.
DcpSST	CAP pull low	Decoupling: Internally generated 1.5 V powered off of Suspend Well. This signal requires decoupling. Decoupling is required even if this feature is not used.
DcpSus	2 CAP pull low TP	1.05 V Suspend well power. Internal VR mode (INTVRMEN sampled high): Well generated internally. Pins should be left No Connect External VR mode (INTVRMEN sampled low): Well supplied externally. Pins should be powered by 1.05 Suspend power supply. Decoupling capacitors are required. NOTE: External VR mode applies to Mobile Only.
DcpSusByp	TP	Internally generated 1.05 V Deep S4/S5 well power. This rail should not be supplied externally. NOTE: No decoupling capacitors should be used on this rail.
V5REF	VCC/VCC3	Reference for 5 V tolerance on core well inputs. This power may be shut off in S3, S4, S5 or G3 states.
V5REF_Sus	5VDUAL/3VDUAL	Reference for 5 V tolerance on suspend well inputs. This power is not expected to be shut off unless the system is unplugged.
VccCore	VCC1_05_PCH	1.05 V supply for core well logic. This power may be shut off in S3, S4, S5 or G3 states.
Vcc3_3	VCC3	3.3 V supply for core well I/O buffers. This power may be shut off in S3, S4, S5 or G3 states.
VccASW	VCC1_05_ME	1.05 V supply for the Active Sleep Well. Provides power to the Intel® ME and integrated LAN. This plane must be on in S0 and other times the Intel ME or integrated LAN is used.

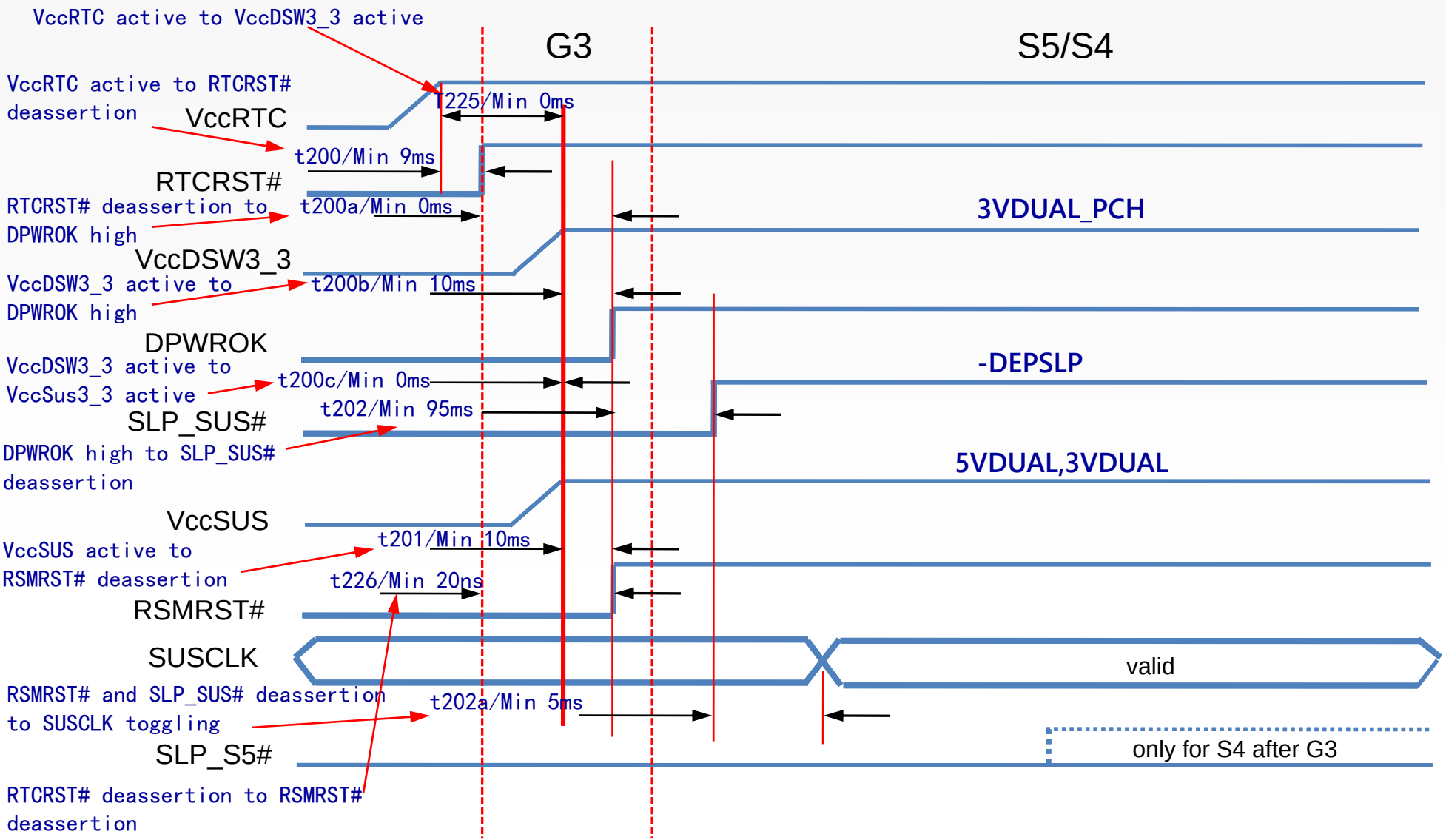
Power and Ground Signals

Name	Power	Description
VccDMI	CPU_VTT	Power supply for DMI. 1.1 V or 1.05 V based on the processor used. Please refer to the respective processor documentation to find the appropriate voltage level.
VccDIFFCLKN	VCC1_05_PCH	1.05 V supply for Differential Clock Buffers. This power is supplied by the corewell.
VccRTC	RTCVDD	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well. This power is not expected to be shut off unless the RTC battery is removed or completely drained. NOTE: Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS can be done by using a jumper on RTCRST# or GPI.
VccIO	VCC1_05_PCH	1.05 V supply for core well I/O buffers. This power may be shut off in S3, S4, S5 or G3 states.
VccSus3_3	3VDUAL	3.3 V supply for suspend well I/O buffers. This power is not expected to be shut off unless the system is unplugged.
VccSusHDA	3VDUAL	Suspend supply for Intel® HD Audio. This pin can be either 1.5 or 3.3 V.
VccVRM	VCC1_8_PCH	1.5 V/1.8 V supply for internal PLL and VRMs
VccDFTERM	VCC1_8_PCH	1.8 V or 3.3 V supply for DF_TVS. This pin should be pulled up to 1.8 V or 3.3 V core.
VccADPLLA	VCC1_05_PCH	1.05 V supply for Display PLL A Analog Power. This power is supplied by the core well.
VccADPLLB	VCC1_05_PCH	1.05 V supply for Display PLL B Analog Power. This power is supplied by the core well.
VccADAC	VCC3_DAC	3.3 V supply for Display DAC Analog Power. This power is supplied by the core well.

Power and Ground Signals

Name	Power	Description
VccAClk	NC	1.05 V Analog power supply for internal clock PLL. This power is supplied by the core well. NOTE: This pin can be left as no connect
VccAPLLEXP	NC	1.05 V Analog Power for DMI. This power is supplied by the core well. NOTE: This pin can be left as no connect
VccAPLLDMI2	NC	1.05 V Analog Power for internal PLL. This power is supplied by core well. NOTE: This pin can be left as no connect
VccAFDIPLL	NC	1.05 V analog power supply for the FDI PLL. This power is supplied by core well. NOTE: This pin can be left as no connect
VccAPLLSATA	NC	1.05 V analog power supply for SATA PLL. This power is supplied by core well. This rail requires an LC filter when power is supplied from an external VR. NOTE: This pin can be left as no connect
V_PROC_IO	CPU_VTT	Powered by the same supply as the processor I/O voltage. This supply is used to drive the processor interface signals. Please refer to the respective processor documentation to find the appropriate voltage level.
VccDSW3_3	3VDUAL_PCH	3.3 V supply for Deep S4/S5 wells. If platform does not support Deep S4/S5 then tie to VccSus3_3.
VccSPI	VCC3_ME	3.3 V supply for SPI Controller Logic. This rail must be powered when VccASW is powered. NOTE: This rail can be optionally powered on 3.3 V Suspend power (VccSus3_3) based on platform needs.
VccSSC	VCC1_05_PCH	1.05 V supply for Integrated Clock Spread Modulators. This power is supplied by core well.
VccClkDMI	VCC1_05_PCH	1.05 V supply for DMI differential clock buffer

G3 w/RTC Loss to S4/S5 (Without Deep Sx Support) Timing Diagram



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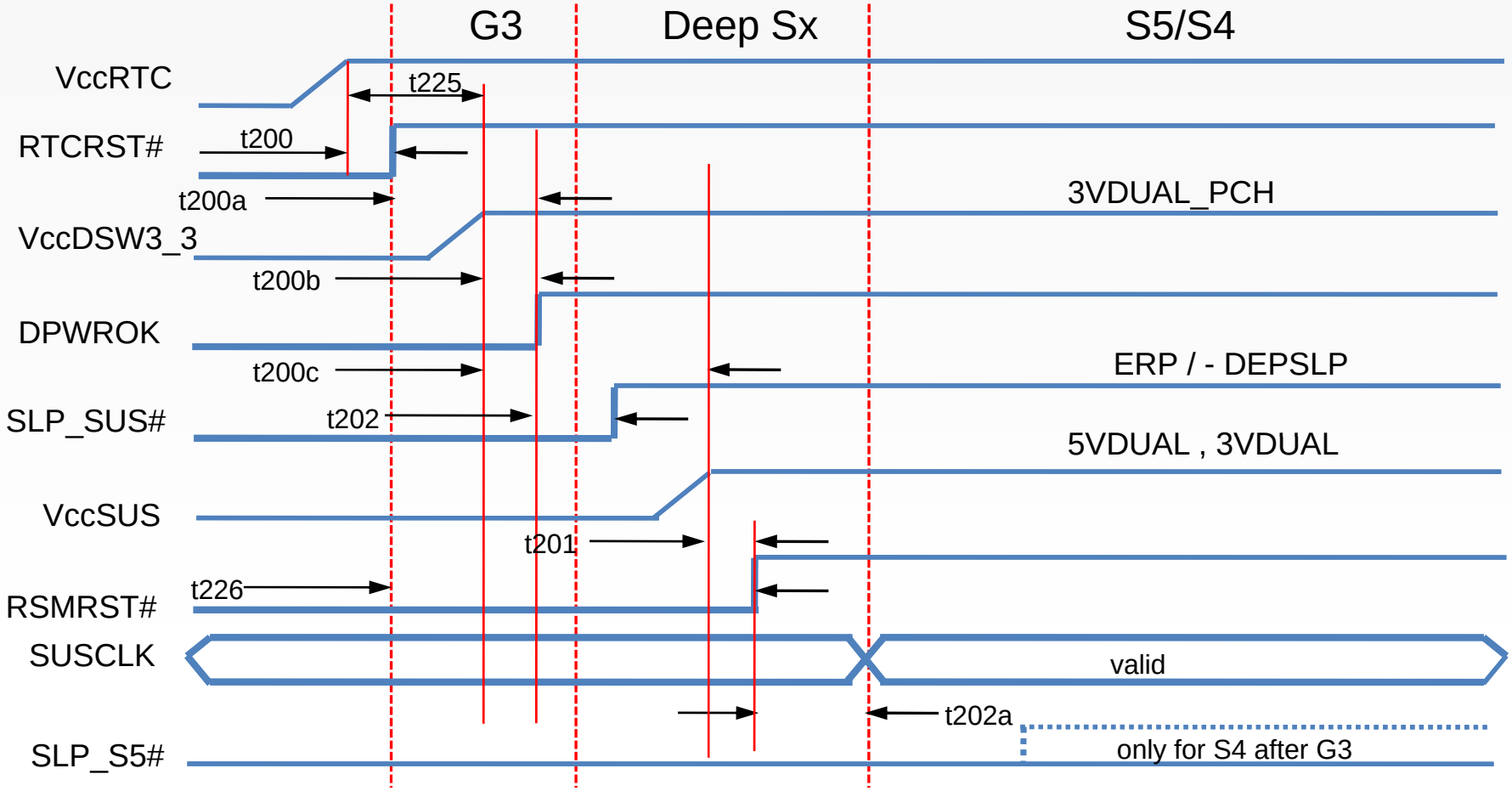
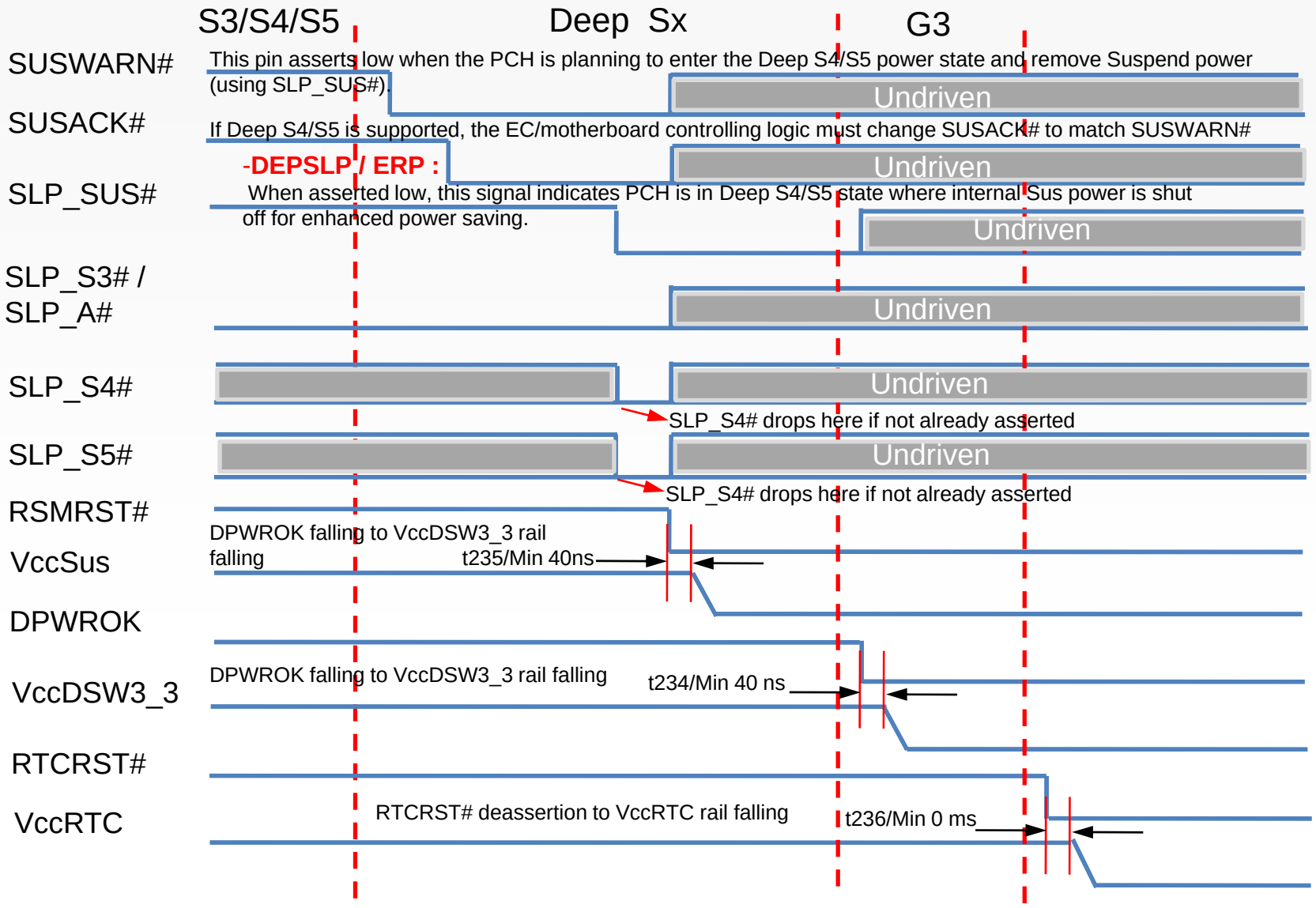
G3 w/RTC Loss to S4/S5 (With Deep Sx Support) Timing Diagram



Note: VccSus rail ramps up later in comparison to VccDSW3_3 due to assumption that SLP_SUS# is used to control power to VccSus.

S3/S4/S5 to Deep Sx to G3 w/ RTC Loss Timing Diagram



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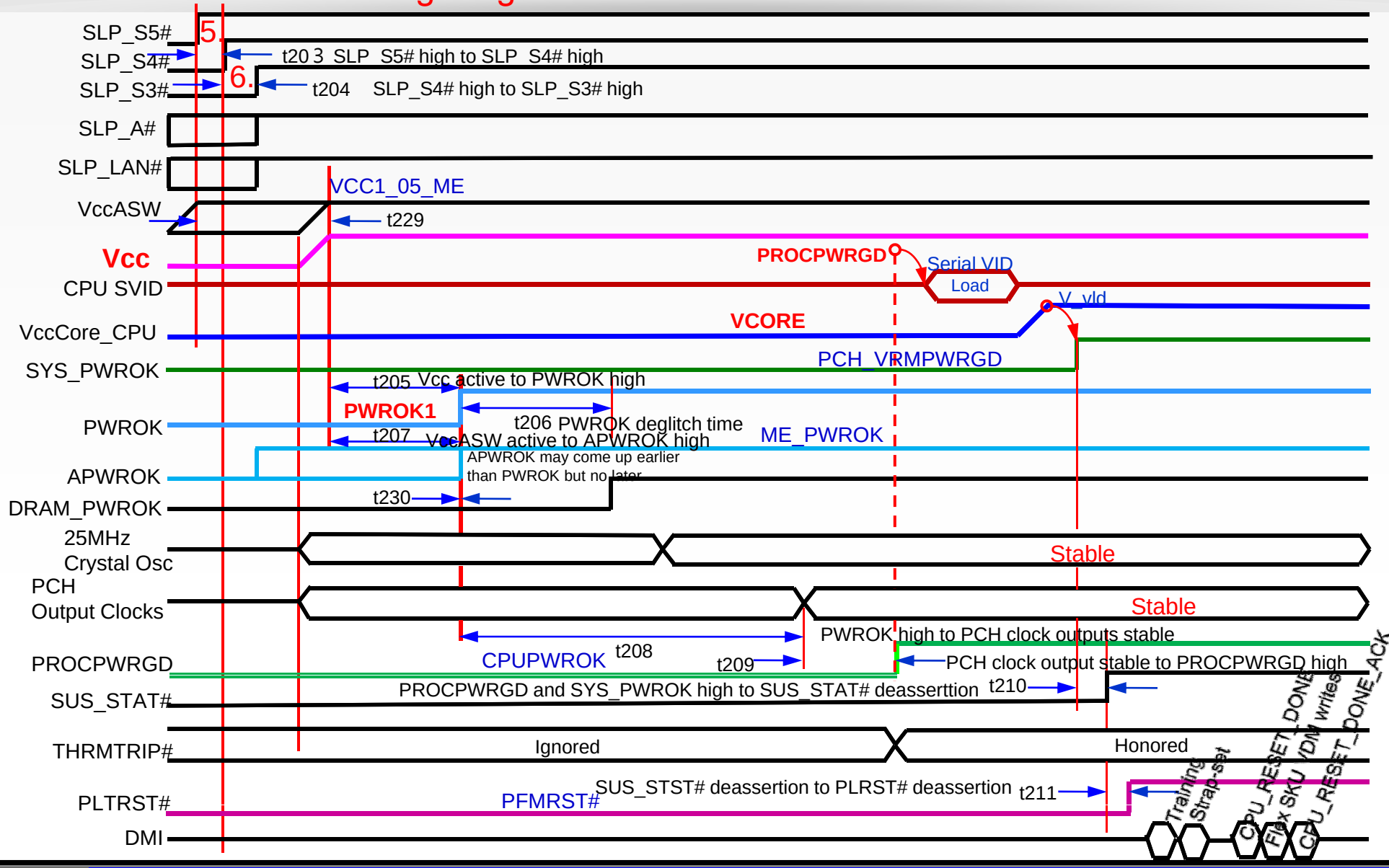
H61 Power Sequence Timing

S5 to S0 Timing Diagram :



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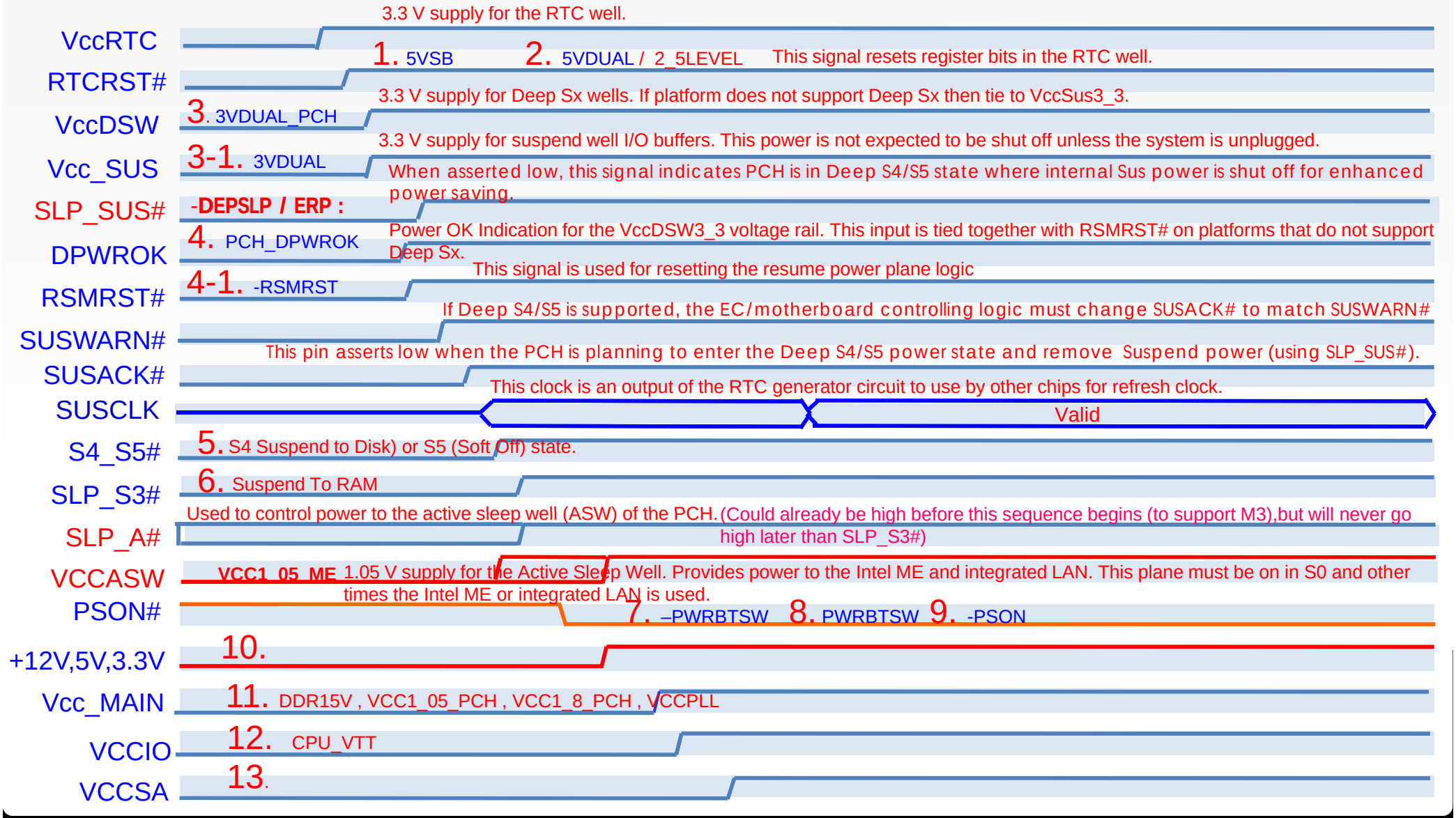
Power Sequencing and Timings (1)



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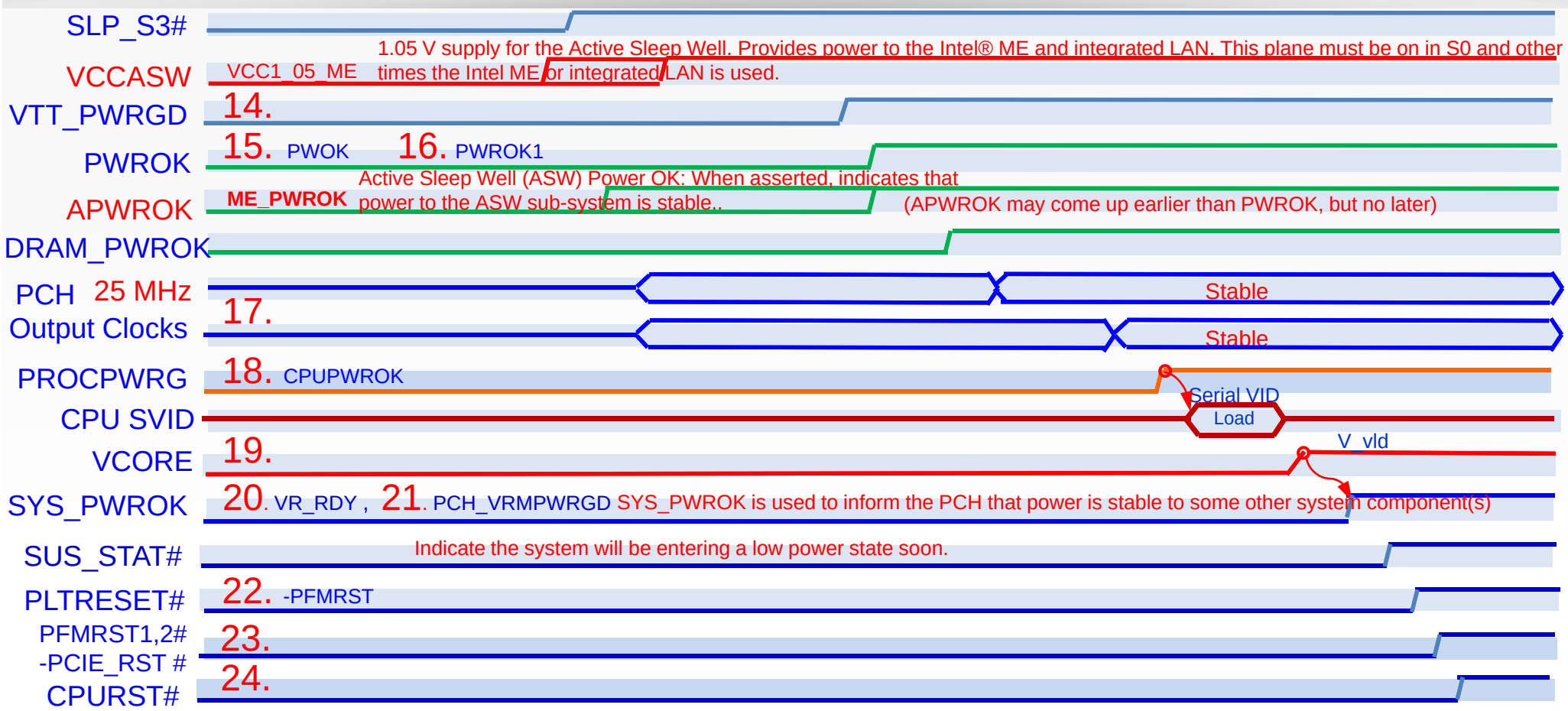
Power Sequencing and Timings (2)



Notes : In the functional operating mode after RTCRST# deasserts for signals in the RTC well, after RSMRST# deasserts for signals in the suspend well, after PWROK asserts for signals in the core well, after DPWROK asserts for Signals in the Deep Sx well, after APWROK asserts for Signals in the Active Sleep well .

S5/Moff-S5/M3 Timing Diagram