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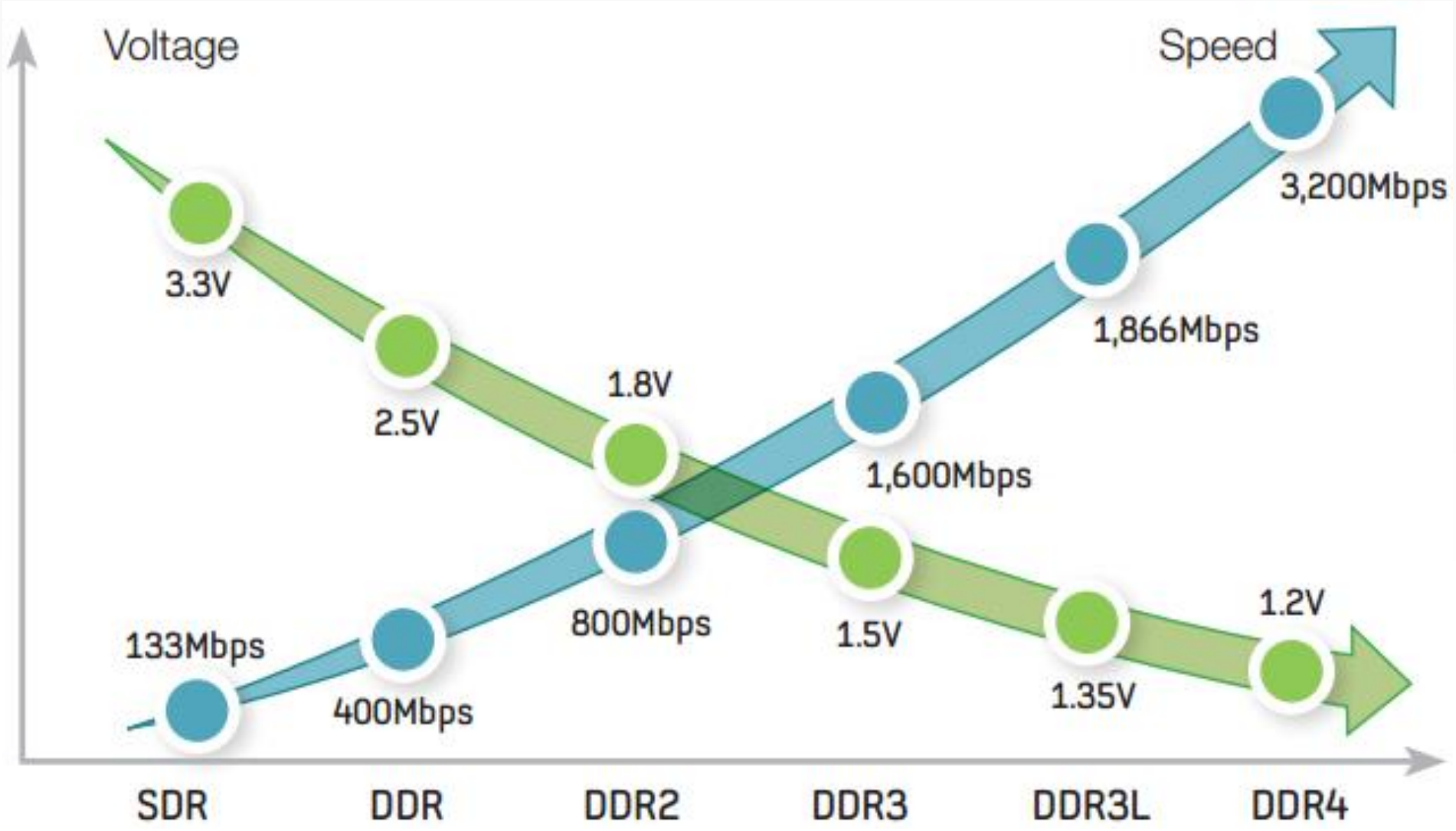
DDR4 Introduction

Engineering 2014/12/25

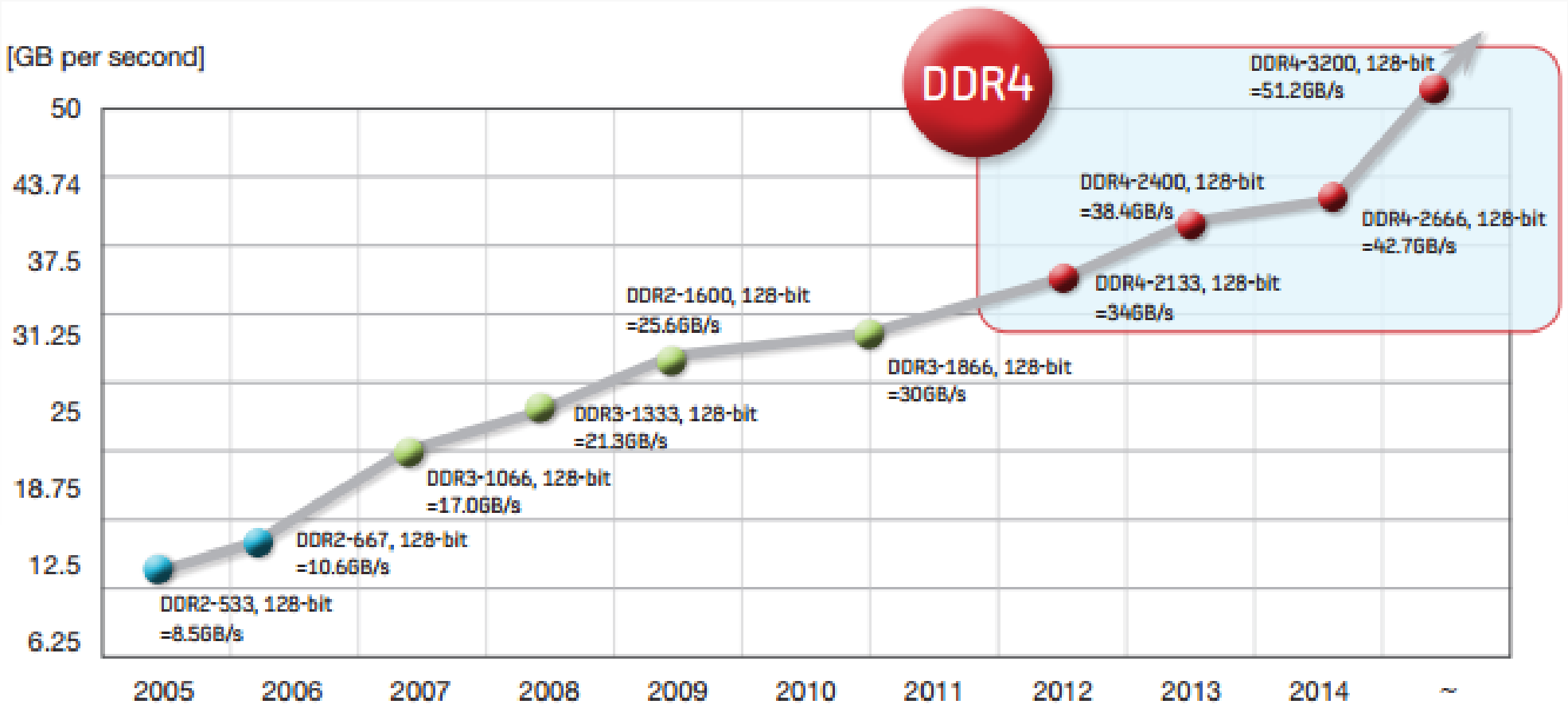
DDR4 SDRAM

DDR4 SDRAM, an abbreviation for double data rate fourth generation synchronous dynamic random-access memory, is a type of synchronous dynamic random-access memory (SDRAM) with a high bandwidth ("double data rate") interface.
It is not compatible with any earlier type of random access memory (RAM) due to different signaling voltages, physical interface and other factors.

DDR Comparison



DDR Comparison



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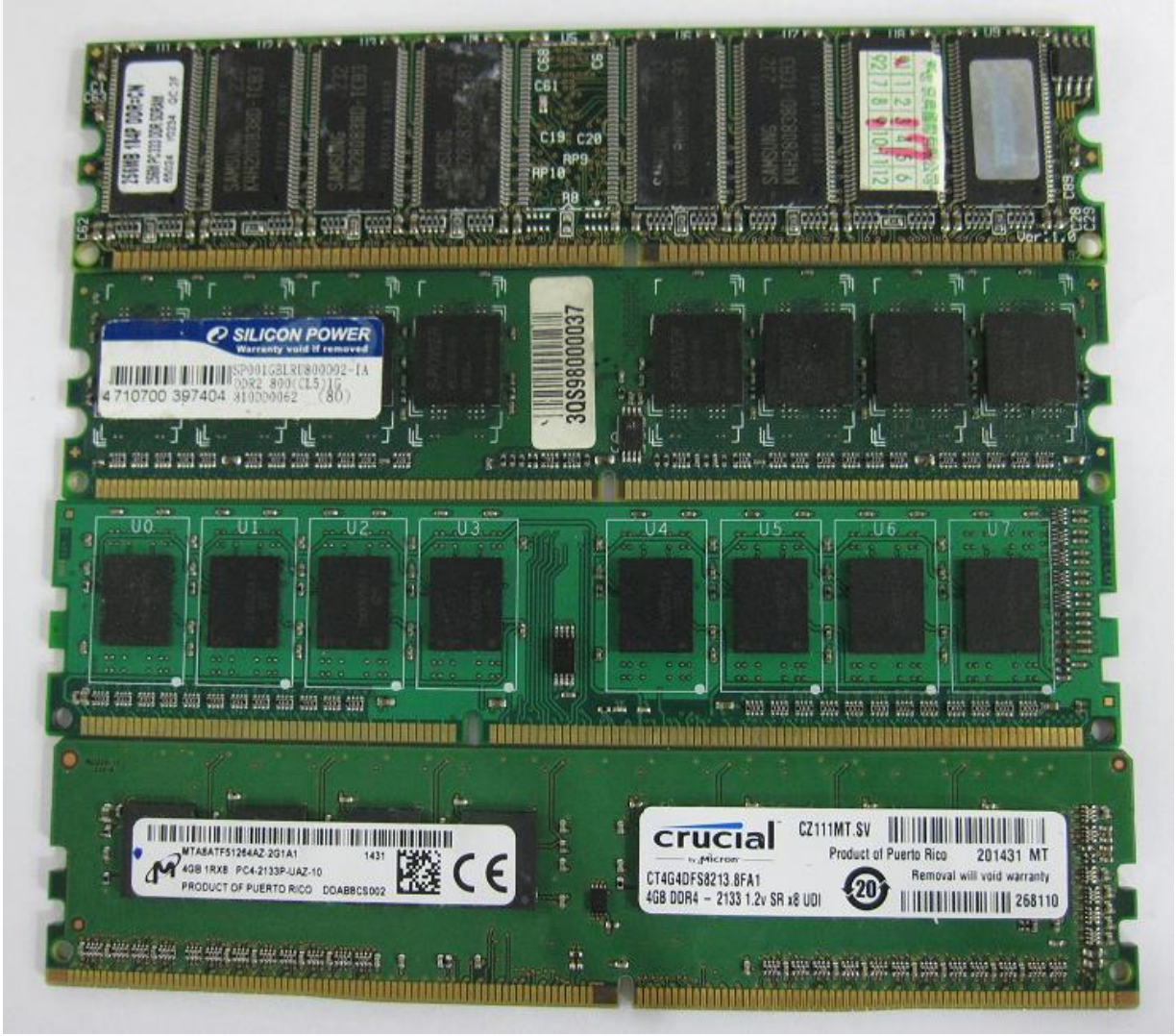
Compare pin DDR



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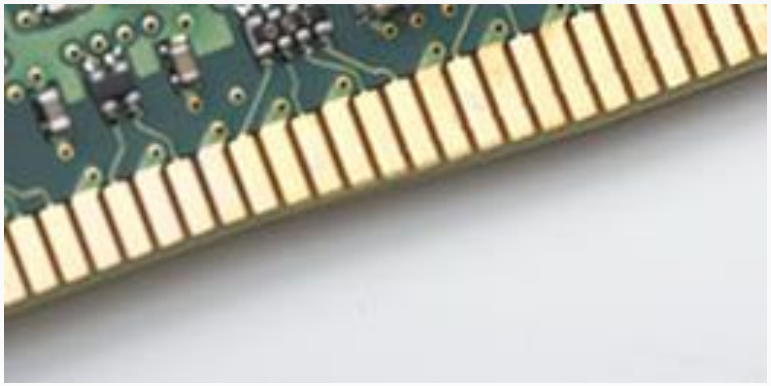
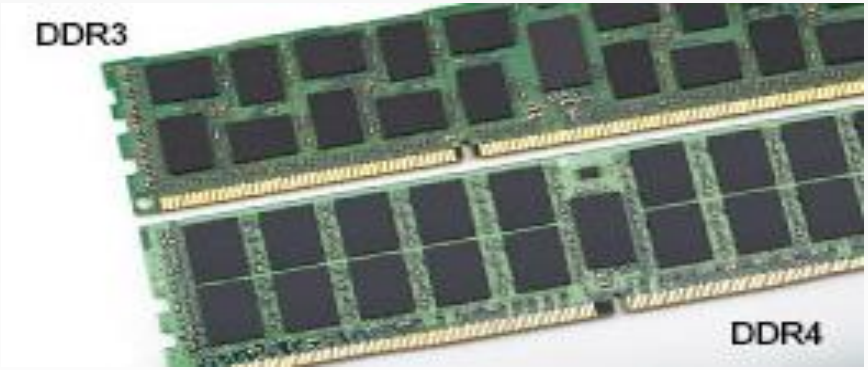
DDR3,4 Comparison



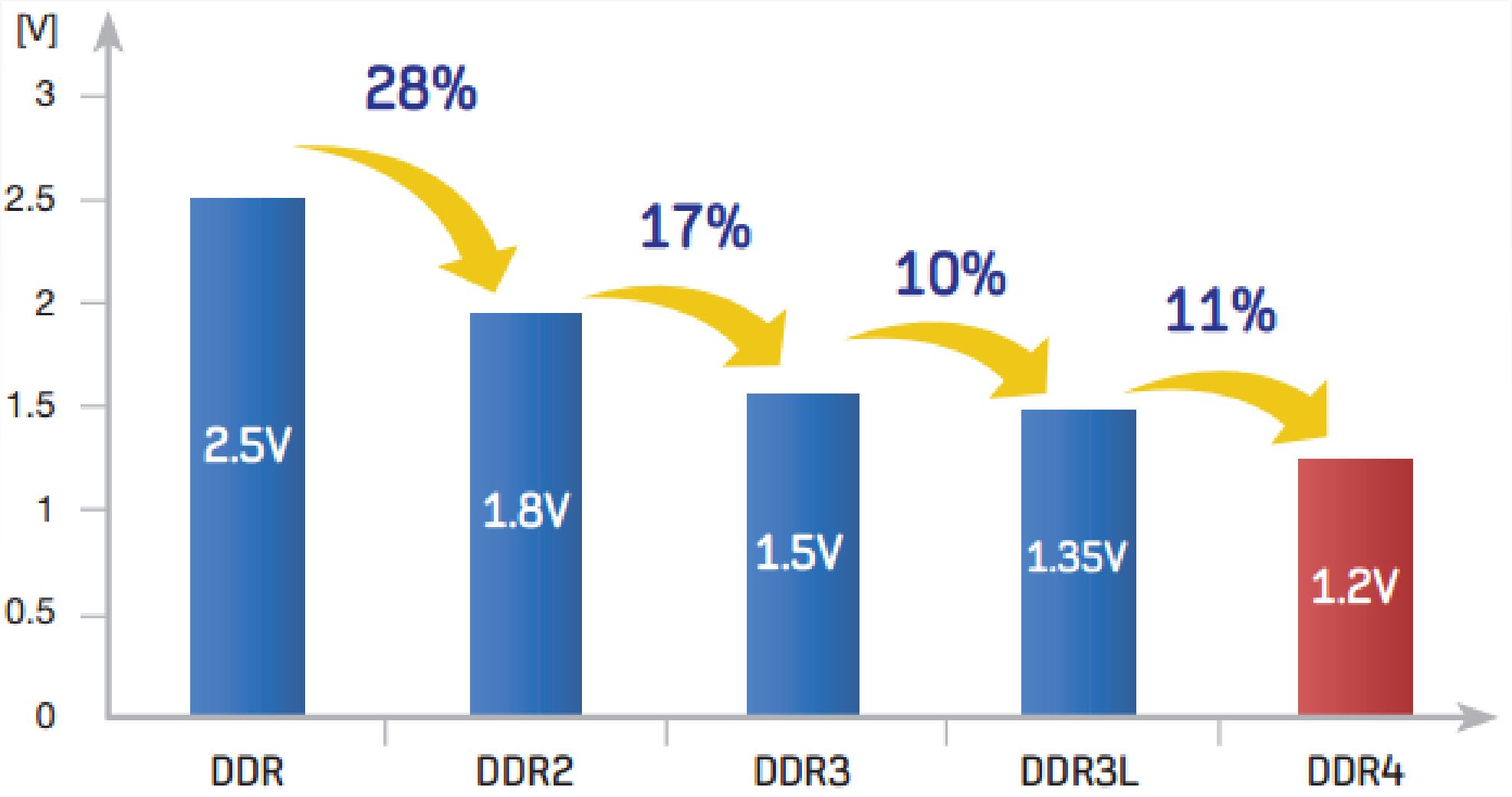
Curved-edge



key-notch-difference

Increased-thickness

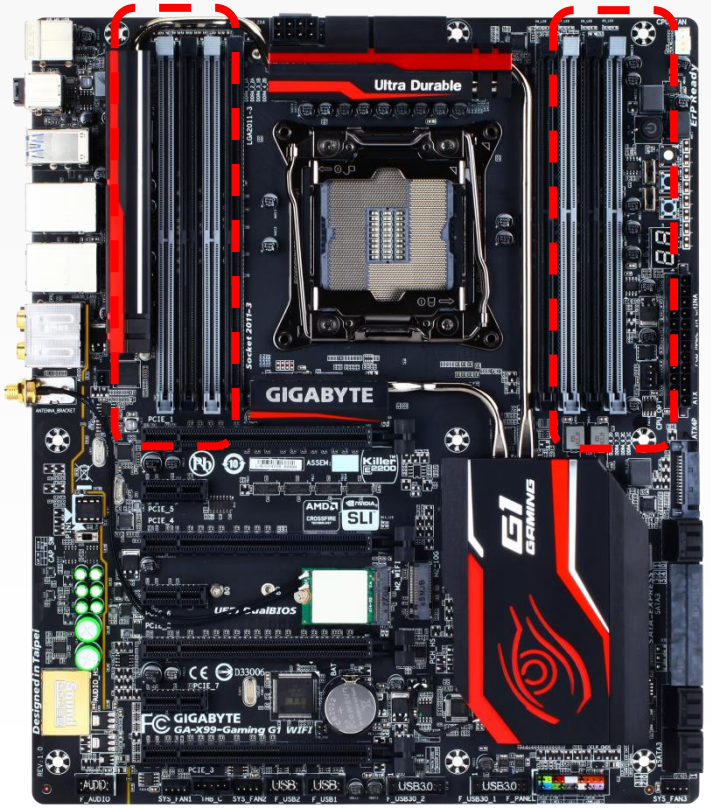
Compare Voltage DDR



4 Channel DDR4

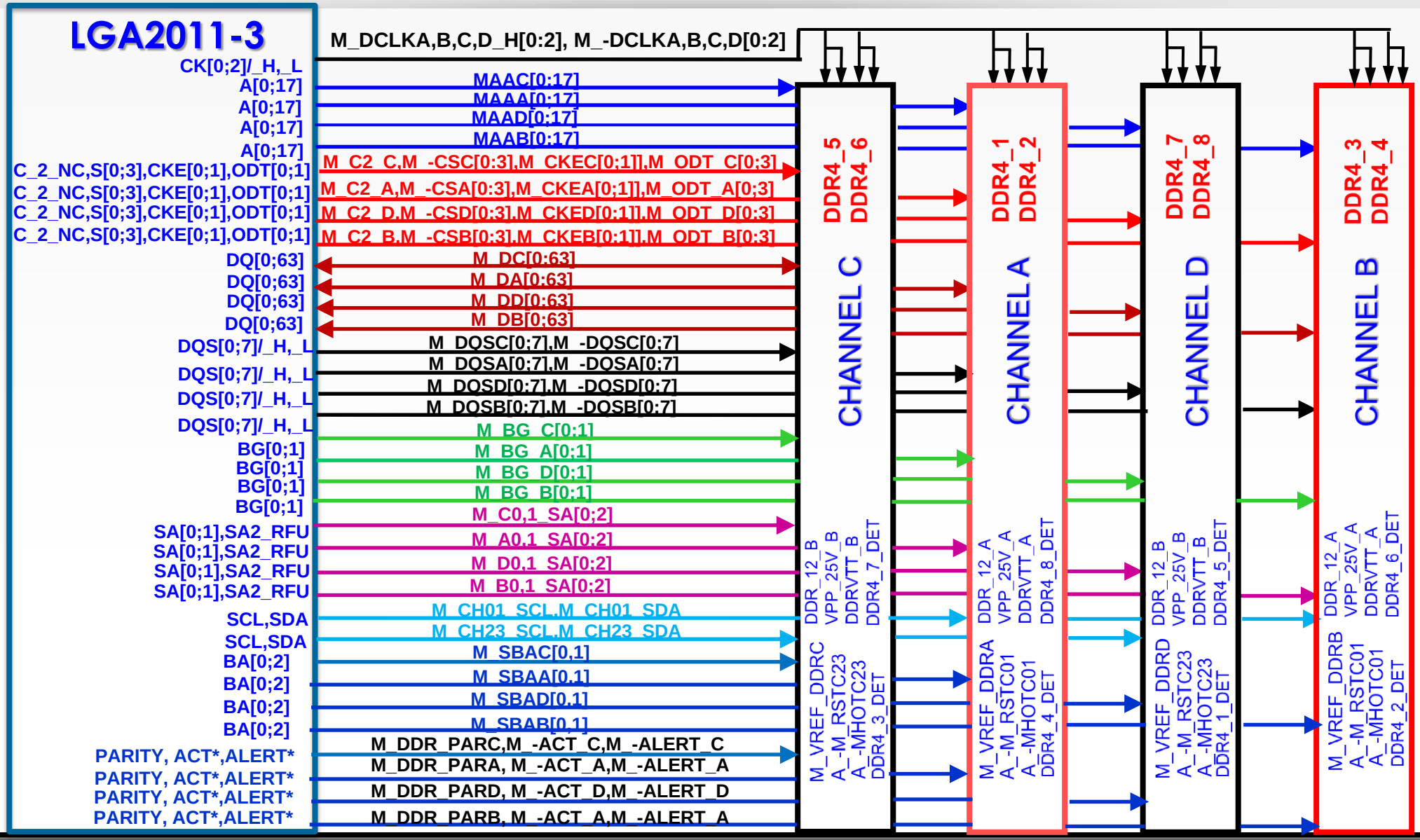
1. Introduction :

The next generation of DRAM is here with DDR4. Featuring stock frequencies starting at 2133 MHz, DDR4 delivers up to 20% less energy consumption and twice as much density as the previous generation DDR3. DDR4 can help GIGABYTE X99 users to load their programs faster, increase responsiveness of their system and help them to handle heavy data tasks in a flash. GIGABYTE X99 motherboards provide 4 Channel DDR4 memory support across the entire range, bringing exceptionally fast memory access.



- 1.2V VDDQ : lower power
- 288 pin DIMM Connector : improved signal to ground ratio, 0.85 mm pin pitch
- 16 banks : performance
- New power features : fine grain refresh control,Temp controlled refresh
- Data bus signaling enhancement : per DRAM addressability ,
  ODT improvements , VDDQ termination , External Vpp.
- Vpp : DRAM activating power supply (2.5V)

X99-Gaming G1-WIFI DDR4- 4 Channel Memory



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DRAM3,4 Technology Comparison

	DDR3	DDR4
Voltage	1.5 V / 1.35 V	1.2V
Strobe	Bi-directional differential	Bi-directional differential
Strobe Configuration	Per byte	Per byte
READ Data Capture	Strobe based	Strobe based
Data Termination	VDDQ/2	VDDQ
Address/Command Termination	VDDQ/2	VDDQ/2
Burst Length	BC4,8	BC4,8
Bank Grouping	No	4
On-Chip Error Detection	No	Command / address parity
		CRC for data bus
Configuration	x4, x8, x16	x4, x8, x16
Package	78-ball / 96-ball FBGA	78-ball / 96-ball FBGA
Data Rate (Mbps/Pin)	800 – 2,133	1,600 – 3,200+
Component Density	1 GB – 8 GB	2 GB – 16 GB
Stacking Options	DDP, QDP	Up to 8H (128-GB stack); single load

DDR4 Processor Signal Groups

Group	Signal Name	Description
Source- Synchronous Signals Data	DDR{0/1/2/3}_DQ[63:00]	Data bus
	DDR{0/1/2/3}_DQS_{DP/DN}[7:00]	Differential data strobes
	DDR{0/1/2/3}_ECC[7:0]	ECC check bits1
Source Clocked Signals Control/ Command/ Address	DDR{0/1/2/3}_MA[17,13:00]	Memory address2
	DDR{0/1/2/3}_BA[1:0]	Bank address (Bank Select)
	DDR{0/1/2/3}_RAS_N/MA[16]	Row address select/Memory Address
	DDR{0/1/2/3}_CAS_N/MA[15]	Column address select/Memory Address
	DDR{0/1/2/3}_WE_N/MA[14]	Write enable/Memory Address
	DDR{0/1/2/3}_ACT_N	Activate
	DDR{0/1/2/3}_BG[1:0]	Bank Group
	DDR{0/1/2/3}_PAR	Command and Address parity3
	DDR{0/1/2/3}_CKE[5:0]	Clock Enable
	DDR{0/1/2/3}_CS_N[9:8, 5:4, 1:0]	Chip select, one per device rank5
	DDR{0/1/2/3}_ODT[5:0]	On-die termination enable
	DDR{0/1/2/3}_C[4:0]	Chip ID

DDR4 Processor Signal Groups

Group	Signal Name	Description
Clocks	DDR{0/1/2/3}_CLK_{DP/DN}[3:0]	Differential clock
Miscellaneous	TEST(3:0)	
	DDR_SCL_C{01/23}	Used for interfacing to the DIMM Serial Presence Detect (SPD)
	DDR_SDA_C{01/23}	
	DDR(01/23}_VREF	Voltage reference for CMD/ADD to the DIMMs.
	DDR{0/1/2/3}_ALERT_N	Parity Error Detected by DIMM
	DDR_RESET_C{01/23}_N	System memory reset: Reset signal from processor to DRAM devices on the DIMMs
	MEM_HOT_C{01/23}_N	Memory throttle control signal.6
	DRAM_PWR_OK_C{01/23}	Power good signal to DRAM in DIMMs