H61 Interface	Check Points	Type	Power	Detail points	Location	Signals Description	Defect Condition
VOLTAGE	RTCVDD	PWR	3.1V	VCCRTC	BC116	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well	No power
	3VDUAL_PCH	PWR	3.3V	VCCDSW3_3	PCH	3.3 V supply for Deep Sx wells. If platform does not support DeepSx then tie to VccSus3_3	No power
	5VDUAL	PWR	5V	V5REF_SUS	R219,BC100	Reference for 5 V tolerance on suspend well inputs	No power
	3VDUAL	PWR	3.3V	VCCSUS3_3	PCH	3.3 V supply for suspend well I/O buffers	No power
				VCCSUSHDA	PCH	Suspend supply for Intel® HD Audio	
				V5REF_SUS	Q26 PIN3	Reference for 5 V tolerance on suspend well inputs	
	VCC3	PWR	3.3V	VCC3_3	PCH	3.3 V supply for core well I/O buffers	Power on Shutdown
				V5REF	Q23 PIN3	Reference for 5 V tolerance on core well inputs	
	VCC	PWR	5V	V5REF	R174	Reference for 5 V tolerance on core well inputs	
	VCC3_ME	PWR	3.3V	VCCSPI	PCH	3.3 V supply for SPI Controller Logic. This rail must be powered when VccASW is powered	
	VCC3_DAC	PWR	3.3V	VCCADAC	Q22 PIN1/PCH	3.3 V supply for Display DAC Analog Power	Onboard VGA no display
	VCC1_05_PCH	PWR	1.05V	VCCIO	BC104,BC106	1.05 V supply for core well I/O buffers.	F.F.Shutdown
				VCCCORE	BC107,BC109	1.05 V supply for core well logic	
				VCCDIFFCLKN[0;3]	PCH	1.05 V supply for Differential Clock Buffers	
				VCCCLKDMI	PCH	1.05 V supply for DMI differential clock buffer	
				VCCADPLLA	BC76,BC82	1.05 V supply for Display PLL A Analog Power	
				VCCADPLLB	BC77,BC83	1.05 V supply for Display PLL B Analog Power	
				VCCSSC[1,2]	PCH	1.05 V supply for Integrated Clock Spread Modulators	
	VCC1_05_ME	PWR	1.05V	VCCASW	BC118	1.05 V supply for the Active Sleep Well. Provides power to the Intel® ME and integrated LAN. This plane must be on in S0 and other times the Intel ME or integrated LAN is used	F.F.Shutdown
	CPUVTT	PWR	1.05V	V_PROC_IO	PCH	Powered by the same supply as the processor I/O voltage. This supply is used to drive the processor interface signals	F.F.Shutdown
				V_PROC_IO_NCTF	PCH		
				VCCDMI_01,02	BC115	Power supply for DMI	
	VCC1_8_PCH	PWR	1.8V	VCCVRM_1,2,3,4	BC129	1.8 V supply for internal PLL and VRMs	F.F.Shutdown
				VCCTETERM_1	BC128	1.8 V supply for DF_TVS. This pin should be pulled up to 1.8 V	
				VCCTFTERM_2			
CLOCK	OSC 25MHz	CLK	25MHz	XTAL25	X1	Connection for 25 MHz crystal to PCH oscillator circuit	F.F. / No CLK output
	Crystal 32.768KHz	CLK	32.768KHz	RTCX1.2	X2	Crystal Input	No power
	CPUCLK	CLK	100MHz	CLKOUT_DMI_N,P	Emulator	100 MHz PCIe Gen2 specification jitter tolerant differential output to processor.	INSTALL CPU NO VCORE
	ITPCLK	CLK	100MHz	CLKOUT_ITPXDPN.P	Emulator	100 MHz Differential output to processor XDP/ITP connector on platform	No boot
	LPC33	CLK	33MHz	CLKOUT_PCI1	R178	33 MHz outputs to PCI connectors/devices	C1-07 Shutdown
	PCH33	CLK	33MHz	CLKOUT_PCI2	R179	33 MHz outputs to PCI connectors/devices	F.F. shutdown
	LPCCLK48	CLK	48MHz	CLKOUTFLEX3/GPIO67	R185	Configurable as a GPIO or as a programmable output clock which can be configured	C1-07 Shutdown
PWRGD	PCH_DPWROK	I	3.3V	DPWROK	R348	Power OK Indication for the VccDSW3_3 voltage rail. This input is tied together with RSMRST# on platforms that do not support Deep Sx.	No Power
	PWROK1	I	3.3V	PWROK	R152	When asserted, PWROK is an indication to the PCH that all of its core power rails have been stable for 10 ms. PWROK can be driven asynchronously. When PWROK is negated, the PCH asserts PLTRST#.	F.F.
	ME_PWROK	I	3.3V	APWROK	R295	Active Sleep Well (ASW) Power OK	F.F.
	PCH_VRMPWRGD	I	3.3V	SYS_PWROK	DR107	This generic power good input to the PCH isdriven and utilized in a platform-specific manner. While PWROK always indicates that the core wells of the PCH are stable, SYS_PWROK is used to inform the PCH that power is stable	F.F. Shutdown No CLK
	CPUPWROK	O	1V	PROCPWRGD	Emulator	This signal should be connected to the processor's UNCOREPWRGOOD input to indicate when the processor power is valid.	Install CPU no VCORE
	DRAM_PWROK	O	1.5V	DRAMPWROK	R244	The PCH asserts this pin to indicate when DRAM power is stable.	C1
RESET	-RSMRST	I	3.3V	RSMRST#	R412,R115,Q58 PIN3	Resume Well Reset: This signal is used for resetting the resume power plane logic, when deasserted, this signal is an indication that the suspend power wells are stable.	No power
	-PFMRST	O	3.3V	PLTRST#	I/O PIN68	Platform Reset: The PCH asserts PLTRST# to reset devices on the platform (such as SIO, FWH, LAN, processor, etc.). The PCH asserts PLTRST# during power-up and when S/W initiates a hard reset sequence through the Reset Control register (I/O Register CF9h).	Reset Hi / 00 shutdown
	-SYS_RST	I	3.3V	SYS_RST#	R383	System Reset: This pin forces an internal reset after being debounced. The PCH will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms ±2 ms for the SMBus to idle before forcing a reset on the system.	Power off restart
	-KBRST	I	3.3V	RCIN#	I/O PIN76	When the PCH detects the assertion of this signal, INIT# is generated using a VLW message to the processor.	K/B can't soft reset
SMBus	SMBDATA	I/OD	3.3V	SMBDATA	R241	SMBus Data: External pull-up resistor is required.	C1 / F.F.
	SMBCLK	I/OD	3.3V	SMBCLK	R239	SMBus Clock: External pull-up resistor is required.	C1 / F.F.
	GPIO11	I	3.3V	SMBALERT#/GPIO11	RN16,D8 PIN3	SMBus Alert: This signal is used to wake the system or generate SMI#.	
Power Mgnt.	-SLP_S3	O	3.3V	SLP_S3#	I/O PIN102	S3 Sleep Control:Suspend To RAM	No power
	-S4_S5	O	3.3V	SLP_S4#	I/O PIN108	S4,S5 Sleep Control:Suspend to Disk) or S5 (Soft Off) state	
	PWRBTSW	I	3.3V	PWRBTN#	I/O PIN106	The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state, If the system is already in a sleep state, this signal will cause a wake event ,If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state.	No power
	PCIE_WAKE#	I	3.3V	WAKE#	R298	PCI Express* Wake Event: Sideband wake signal on PCI Express asserted by components requesting wake up.	Power off restart
	-DEPSLP	O	3.3V	SLP_SUS#	R4948	Deep Sx Indication: When asserted (low), this signal indicates PCH is in Deep Sx state where internal Sus power is shut off for enhanced power saving. When deasserted (high), this signal indicates exit from Deep Sx state and Sus power can be applied to PCH.	No power
Direct Media Interface	DMI[3;0]TX[P,N]	O	1V	DMI[3;0]TX/TX#[3:0]	LED TESTER	Direct Media Interface Differential Transmit Pair[3;0]	No boot
	DMI[3;0]RX[P,N]	I	1V	DMI[3;0]RX/RX#[3:0]	LED TESTER	Direct Media Interface Differential Receive Pair [3;0]	No boot
Processor Interface	A20GATE	I	3.3V	A20GATE	I/O PIN77 ,R307	A20 Gate: Functionality reserved. A20M# functionality is not supported. This pin requires external pull-up.	
	PMSYNC	O		PM_SYNCH	PCH , CPU	Power Management Sync: Provides state information from the PCH to the processor	
	-KBRST	I	3.3V	RCIN#	I/O PIN76	When the PCH detects the assertion of this signal, INIT# is generated using a VLW message to the processor	K/B can't soft reset
	-THRMTRIP	I	1.2V	THERMTRIP#	RN19,Q25 PIN1	Thermal Trip: When low, this signal indicates that a thermal trip from the processor occurred, and the PCH will immediately transition to a S5 state. The PCH will not wait for the processor stop grant cycle since the processor has overheated.	F.F. shutdown
	CPUPWROK	O	1V	PROCPWRGD	EMULATOR	This signal should be connected to the processor's UNCOREPWRGOOD input to indicate when the processor power is valid.	Install CPU no VCORE
Fan Speed Control	SB_PECI	I/O		PECI	CPU,I/O PIN86	PECI (Platform Environment Control Interface): A serial sideband interface to the processor, it is used primarily for thermal, power, and error management.	F.F. shutdown
	SSTCTL	I/O		SST	I/O PIN84	Simple Serial Transport: Single-wire, serial bus. Connect to SST compliant devices such as SST thermal sensors or voltage sensors.	F.F. shutdown
SPI Interface	-ICH_SPI_CS	O	3.3V	ICS#	BIOS / PIN1	SPI Chip Select 0,1: Used as the SPI bus request signal.	No bbot
	SPI_MISO	I	3.3V	SO	BIOS / PIN2	SPI Master IN Slave OUT: Data input pin for PCH.	No bbot
	ICH_SPI_MOSI	I/O	0V	SI	BIOS / PIN5	SPI Master OUT Slave IN: Data output pin for PCH.	No bbot
	ICH_SPI_CLK	O	CLK	SCK	BIOS / PIN6	SPI Clock: SPI clock signal, during idle the bus owner will drive the clock signal low. 17.86 MHz and 31.25 MHz.	No bbot
LPC Interface	LAD[3:0]	I/O	3.3V	LAD[3:0]	I/O PIN72,73,74,75	LPC Multiplexed Command, Address, Data: For LAD[3:0],	C1 shutdown / 00
	-LFRAME	O	3.3V	LFRAME#	I/O PIN71	LPC Frame: LFRAME# indicates the start of an LPC cycle, or an abort	C1 shutdown / 00
	A20GATE	I	3.3V	A20GATE	I/O PIN77 ,R307	when asserted low forces bit 20 of the physical address to be zero for all on-chip cache or external memory accesses	
	SERIRQ	I/OD	3.3V	SERIRQ	I/O PIN70	Serial Interrupt Request: This pin implements the serial interrupt protocol	Device no work
	-LDRQ	I	3.3V	LDRQ#	I/O PIN69	LPC Serial DMA/Master Request Inputs: LDRQ[1:0]# are used to request DMA or bus master access.	
Msc Signals	INTVRMEN	I	3V	INTVRMEN	I	Internal Voltage Regulator Enable: This signal enables the internal 1.05 V regulators when pulled high.	No power
	DSWVRMEN	I	3V	DSWVRMEN	R237	Deep Sx Well Internal Voltage Regulator Enable: This signal enables the internal DSW 1.05 V regulators.	No power
	-RTCRST	I	3V	RTCRST#	R234	RTC Reset: When asserted, this signal resets register bits in the RTC well	No power
	-SRTCRST	I	3V	SRTCRST#	R229	Secondary RTC Reset: This signal resets the manageability register bits in the RTC well when the RTC battery is removed	No power
System Management Interface	RTCVDD	I	3V	INTRUDER#	R231	Intruder Detect: This signal can be set to disable the system if box detected open. This signal's status is readable, so it can be used like a GPI if the Intruder Detection is not needed	No power
	SML0DATA	I/OD	3.3V	SML0DATA		System Management Link 0 Data: SMBus link to external PHY	
	SML0CLK	I/OD	3.3V	SML0CLK		System Management Link 0 Clock: SMBus link to external PHY	
	GPIO60	O OD	3.3V	SML0ALERT#/GPIO60	RN15	SMLink Alert 0: Output of the integrated LAN controller to external PHY	
	SML1DAT	I/OD	3.3V	SML1DATA	I/O PIN23,RN16	System Management Link 1 Data: SMBus link to optional Embedded Controller or BMC	
	SML1CLK	I/OD	3.3V	SML1CLK	I/O PIN24,RN15	System Management Link 1 Clock: SMBus link to optional Embedded Controller or BMC	
	-PCH_HOT	O OD	3.3V	SML1ALERT#	RN15	SMLink Alert 1: Alert for the ME SMBus controller to optional Embedded Controller or BMC	F.F. shutdown
Real Time Clock Interface	Crystal 32K768Hz	CLK	32.768KHz	RTCX1.2	X2	Crystal Input 1: This signal is connected to the 32.768 kHz crystal	CMOS check sum error / No power
General Purpose I/O Signals	GPIO15,28...	I/O	3.3V	GPIO[72,57,32,28,27,15,8]	Pull high Resistor & Related Circuit	All GPIOs can be configured as either input or output.	No boot,shutdown restart
Testability Signals	TDO,TCK, -TRST TDI,TMS, -HPRDY	I ,OD	1V	TDO,TCK, TRST# TDI,TMS, HPRDY#	RN6,RN19	Test Clock Input(TCK),Test Mode Select (TMS),Test Data Input (TDI),Test Data Output (TDO).	No boot