IT8728F Interface	Check Points	Type	Power	Detail Points	Location	Signals Description	Defect Condition
VOLTAGE	VBAT	PWR	3.1V	VBAT	PIN100	3V Battery Supply	No power
	3VDUAL_PCH / IT_VCCH	PWR	3.3V	3VSB	PIN98	3.3V Standby Power Supply	No power
				3VSB	PIN66	3.3V Standby Power Supply	
				3VSB	PIN35	3.3V Standby Power Supply	
	VCC3 / IT_AVCC	PWR	3.3V	AVCC3	PIN2	3.3V Analog Power Supply	F.F. shutdown
	3VDUAL / 28_3VSB	PWR	3.3V	SYS_3VSB	R166,PIN97	System 3.3V Standby Power Detector The function of this pin is System Standby Power Detector for RSMRST# output and EuP signal Control	No power
	SIO_18V	PWR	1.8V	VCORE	BC34,PIN67	nternal Power supply(1.8V) It is required to connect this pin with the external capacitance.	Auto Power on
CLOCK	LPC33	CLK	33MHz	PCICLK	PIN78	PCI Clock 33 MHz PCI clock input for LPC I/F and SERIRQ.	C1-07 Shutdown
	LPCCLK48	CLK	48MHz	CLKIN	PIN80	24 or 48 MHz Clock Input	
PWRGD	PWOK / IO_PWOK	I	3.3V	ATXPG	PIN50	ATX Power Good For PWRGD1/2/3 signal, it is (AVCC3 power-level-detect AND SUSB# AND VIN2(+12V_SEN) AND VIN3(+5V_SEN) AND ATXPG)	F.F.
	PWROK1 / ITE_PWROK1	O	3.3V	PWRGD1	R152 / PIN63	Power Good Output 1 with 30ms Delay Time For PWRGD1/2/3 signal, it is (AVCC3 power-level-detect AND SUSB# AND VIN2(+12V_SEN) AND VIN3(+5V_SEN)AND ATXPG).	F.F.
RESET	-RSMRST	O	3.3V	RSMRST#	R115 / PIN116	Resume Reset # The first function of this pin is Resume Reset #. It is a power good signal of 3VSB.	No power
	-PFMRST	I	3.3V	LRESET#	PIN68	LPC RESET # EC block will not be reset by LRESET#, which is controlled by AVCC3 PWRGD	Reset Hi / 00 shutdown
	-PFMRST1 / PRST1	O	3.3V	PCIRST2	R161 / PIN65	PCI Reset 1 # The first function of this pin is PCI Reset 1 #. which is a buffer of LRESET#.	Reset Hi / 00 shutdown
	-PFMRST2 / PRST2	O	3.3V	RCIN#	R4938 / PIN64	PCI Reset 2 # The first function of this pin is PCI Reset 2 #, which is a buffer of LRESET# / PCIRSTIN#.	Reset Hi / 00 shutdown
	-PCIE_RST	O	3.3V	PCIRST3	R121 / PIN115	PCI Reset 3 # The first function of this pin is PCI Reset 3 #. which is a buffer of LRESET#.	Device fail
	-KBRST	O	3.3V	KRST#	PIN76	Keyboard Reset #	K/B can't soft reset
Power On Strapping Options	JP2	O	3.3V	RTS1#/JP2	R65 /PIN25	1 : Disable WDT to rest PWROK 0 : Enable WDT to rest PWROK	No boot
	JP3	O	3.3V	SOUT1#/JP3	R80 / PIN27	1 : The default value of EC Index 63h/6Bh/73h is 80h 0 : The default value of EC Index 63h/6Bh/73h is 00h	No boot
	JP4	O	3.3V	DTR1#/JP4	R63 / PIN29	1 : Disable K8 power sequence function 0 : Enable K8 power sequence function	No boot
System Management Interface	SML1DAT	I/OD	3.3V	VLDT_EN	PIN23	System Management Link 1 Data: SMBus link to optional Embedded Controller or BMC.	
	SML1CLK	I/OD	3.3V	VCORE_EN	PIN24	System Management Link 1 Clock: SMBus link to optional Embedded Controller or BMC.	
Power Mgnt.	-SLP_S3	I	3.3V	SUSB#	PIN102	S3 Sleep Control:Suspend To RAM	No power
	-S4_S5	I	3.3V	SUSC#	PIN108	S4,S5 Sleep Control:Suspend to Disk) or S5 (Soft Off) state	
	-PWRBTSW	I	3.3V	PANSWH#	PIN106	Main Power Switch Button Input #	No power
	PWRBTSW	O	3.3V	PWRON#	PIN103	Power On Request Output # The first function of this pin is Power On Request Output #,when the Internal 3VSB-OK is ready, the Hi/Lo status of PWRON# will be detected. 1: RSMRST# output is detected by 3VSB 0: RSMRST# output is detected by SYS_3VSB (pin70)	No power
	-PSON	O	0V	PSON#	PIN107	Power Supply On-Off Output #	No power
	ERP	O	5V	GP66	PIN22	Energy-related Products	No power
	-5VSB_CTRL	O	5V	5VSB_CTRL#	PIN47	5VSB_CTRL# Power Control Signal	No power
SPI Interface	HOLD_M-	I/O	3.3V	HOLD_M#	PIN36	Dual BIOS signal HOLD_M#	No boot
	HOLD_B-	I/O	3.3V	HOLD_B#	PIN37	Dual BIOS signal HOLD_B#	No boot
PCH / LPC Interface	LAD[3:0]	I/O	3.3V	LAD[3:0]	PIN72,73,74,75	LPC Address / Data 0-3 4-bit LPC address/bi-directional data lines.	C1 shutdown / 00
	-LFRAME	I	3.3V	LFRAME#	PIN71	LPC Frame # This signal indicates the start of the LPC cycle.	C1 shutdown / 00
	A20GATE	O	3.3V	GA20	PIN77	when asserted low forces bit 20 of the physical address to be zero for all on-chip cache or external memory accesses	No boot
	SERIRQ	I/O	33V	SERIRQ	PIN70	Serial Interrupt Request: This pin implements the serial interrupt protocol	Device no work
	-LDRQ	O	3.3V	LDRQ#	PIN69	LPC Serial DMA/Master Request Inputs: LDRQ[1:0]# are used to request DMA or bus master access.	Device no work
	-LPCPME	O	3.3V	PME#	PIN104	Power Management Event # The first function of this pin is Power Management Event #. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from the D3 (cold) state.	Poweer off restart
Power OC Interface	VCORE_OV1,2	O		GP27,GP28	PIN51,52	CPU VCORE OC	F.F. shutdown
	DDR_OV1,2,3	O		GP20,21,22	PIN56,57,58	Memory DDR15V OC	
	VTT_OV1,2	O		GP25,24	PIN53,54	CPU_VTT OC	
	VTT_LEVEL	I	2.5V	GP37	R104/PIN42	CPU_VTT LEVEL detect	
Monitor Interface	VIN2	I	2.0V	VIN2(+12V)	PIN127	Voltage Analog Input 2 (+12V power detector) ,The function of this pin is 0 to 3.072V FSR Analog Input,Besides, it is the power detector for PWRGD1/2/3.	Reset Hi /PWROK1 no output
	VIN3	I	2.0V	VIN3(+5V)	PIN126	Voltage Analog Input 3 (+5V power detector) ,The function of this pin is 0 to 3.072V FSR Analog Input,Besides, it is the power detector for PWRGD1/2/3.	Reset Hi / PWROK1 no output
	VIN0,1,5,6	I	1.05V 2.0V	VIN0,1,5,6	PIN1,128124,123	Voltage Analog Input 0,1,5,6	
	TEMP3	I	2.8V	TMPIN3	PIN119	External Thermal Inputs 3 ,these pins are connected to thermistors 3 or thermal temperature sensors	F.F. shutdown
	DDR_TEMP	I	2.8V	TMPIN2	PIN120	External Thermal Inputs 2 ,these pins are connected to thermistors 3 or thermal temperature sensors	
	SYS_TEMP	I	1.2V	TMPIN1	PIN121	External Thermal Inputs 1 ,these pins are connected to thermistors 3 or thermal temperature sensors	
	-THERM	I	3,3V	PCIRSTIN#/CIRTX2/GP15	Q14 PIN3 /Q10 PIN3 / PIN34	In the event of a catastrophic cooling failure, the processor will automatically shutdown when the silicon has reached a temperature above the maximum Tc	
	VREF	O	2.8V	VREF	PIN122	Reference Voltage Output (2.8V) Regulated and referred voltage for external temperature sensors and negative voltage monitors	C1-F.F.
Fan Speed Control	PECI	I		PECI	CPU, PIN86	PECI (Platform Environment Control Interface): A serial sideband interface to the processor, it is used primarily for thermal, power, and error management	F.F. shutdown
	PECI_CTL	O		PCH_C1/GP14	R145,PIN62	Platform Environment Control Interface Control	F.F. shutdown
	SSTCTL	I		SST	PCH,PIN84	Simple Serial Transport: Single-wire, serial bus. Connect to SST compliant devices such as SST thermal sensors or voltage sensors	F.F. shutdown
COM Port Interface	RTS1-...CTS1-	I,O	5V 3.3V	RTS1-...CTS1-16	GD75232	COM port signals connects to GD75232 PIN12~PIN19	No boot
LAN Interface	ISOLAT	O	0.8V	GP17/RI2#	PIN59,LAR4,5	Used to isolate the RTL8111F from the PCI Express bus.	Can't detect LAN chip