| 1155 Interface | Check Points | Type | Power | Detail Points | Location | Signals Description | Defect Condition |
|---|---|---|---|---|---|---|---|
| VOLTAGE | VCORE | Ref | 1.0V | VCC | Emulator | Processor core power rail | F.F. shutdown |
| | CPU_VTT | Ref | 1.0V | VCCIO | Emulator | Processor power for I/O. | F.F. shutdown |
| | DDR_15V | Ref | 1.5V | VDDQ | Emulator | Processor I/O supply voltage for DDR3 | F.F. |
| | CPU_VAXG | Ref | 0.9V | VCCAXG | Emulator | Graphics core power supply | Hang 25 |
| | VCCPLL | Ref | 1.8V | VCCPLL | Emulator | VCCPLL provides isolated power for internal processor PLLs | INSTALL CPU NO VCORE |
| | VCCSA | Ref | 0.9V | VCCSA | Emulator | System Agent power supply | F.F. shutdown |
| CLOCK | CPUCLK | Diff CLK | 100MHz | BCLK | Emulator | Differential bus clock input to the processor | INSTALL CPU NO VCORE |
| | ITPCLK | Diff CLK | 100MHz | BCLK_ITP | Emulator | These signals are connected in parallel to the top side debug | No Boot |
| PWRGD | CPUPWROK | I | 1.0V | UNCOREPWRGOOD | Emulator | The processor requires this input signal to be a clean indication | INSTALL CPU NO VCORE |
| | DRAM_PWROK | I | 1.5V | SM_DRAMPWROK | Emulator | that the VCCSA, VCCIO, VAXG, and VDDQ, power supplies are | C1 |
| RESET | -CPURST | I | 1.1V | RESET# | Emulator | Platform Reset pin driven by the PCH. | Reset Hi |
| | -DDR3_RST | O | 0V | SM_DRAMRST# | Emulator | DDR3 DRAM Reset: Reset signal from processor to DRAM devices. | C1 |
| Power Signals | VIDSOUT<br>VIDSCLK<br>-VIDALERT | O<br>O I | 1.05V | VIDSOUT<br>VIDSCLK<br>VIDALERT# | Emulator | VIDALERT#, VIDSCLK, and VIDSCLK comprise a three signal serial synchronous interface used to transfer power management information between the processor and the voltage regulator controllers. This serial VID interface replaces the parallel VID interface on previous processors | No VCORE |
| Sense Signals | VCC_SENSE<br>VSS_SENSE | O | 1.0V<br>0V | VCC_SENSE<br>VSS_SENSE | DR466<br>DR468 | VCC_SENSE and VSS_SENSE provide an isolated, low impedance connection to the processor core voltage and ground. They can be used to sense or measure voltage near the silicon. | F.F. Shutdown |
| | VAXG_SENSE<br>VSSAXG_SENS | O | 1.0V<br>0V | VAXG_SENSE<br>VSSAXG_SENS | DR445<br>DR450 | VAXG_SENSE and VSSAXG_SENSE provide an isolated, low impedance connection to the VAXG voltage and ground. They can be used to sense or measure voltage near the silicon. | F.F. Shutdown |
| | VTT_SENSE<br>VTT_VSS | O | 1.0V<br>0V | VCCIO_SENSE<br>VSS_SENSE_VCCIO | TR67 TR69 | VCCIO_SENSE and VSS_SENSE_VCCIO provide an isolated, low impedance connection to the processor VCCIO voltage and ground. They can be used to sense or measure voltage near the silicon. | F.F. Shutdown |
| | VSA_SENSE | O | 0.9V | VCCSA_SENSE | U1 PIN9 | VCCSA_SENSE provide an isolated, low impedance connection to the processor system agent voltage. It can be used to sense or measure voltage near the silicon. | Hang 25 |
| | VTT_SEL | O | | VCCSA_VID | | Voltage selection for CPU_VTT | |
| | VSA_SEL | O | | VCCIO_SELECT | | Voltage selection for VCCSA | |
| Direct Media Interface DMI | DMI_[3;0]RXN<br>DMI_[3;0]RXP | I | 1V | DMI_RX[3:0]<br>DMI_RX#[3:0] | Emulator | DMI Input from PCH: Direct Media Interface receive differential pair | No Boot |
| | DMI_[3;0]TXN<br>DMI_[3;0]TXP | O | 1V | DMI_TX[3:0]<br>DMI_TX#[3:0] | Emulator | DMI Output to PCH: Direct Media Interface transmit differential pair. | |
| Flexible Display Interface FDI | FDI_FSYNC0 | I | | FDI0_FSYNC[0] | Emulator | LPC Address / Data 0-3<br>4-bit LPC address/bi-directional data lines. | Onboard VGA No Display |
| | FDI_LSYNC0 | I | | FDI0_LSYNC[0] | Emulator | LPC Frame #<br>This signal indicates the start of the LPC cycle. | |
| | FDI_TXP[7;0]<br>FDI_TXN[7;0] | O | | FDI_TX[7:0]<br>FDI_TX#[7:0] | Emulator | when asserted low forces bit 20 of the physical address to be zero for all on-chip cache or external memory accesses | |
| | FDI_FSYNC1 | I | | FDI1_FSYNC[1] | Emulator | Serial Interrupt Request: This pin implements the serial interrupt protocol | |
| | FDI_LSYNC1 | I | | FDI1_LSYNC[1] | Emulator | LPC Serial DMA/Master Request Inputs: LDRQ[1:0]# are used to request DMA or bus master access. | |
| | FDI_INT | I | | FDI_INT | Emulator | Power Management Event #<br>The first function of this pin is Power Management Event #. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from the D3 (cold) state. | |
| | FDI_RCOMP | I | 1.0V | FDI_COMPIO<br>FDI_ICOMPO | Emulator | Intel Flexible Display Interface Compensation | |
| Error and Thermal Protection Signals | PECI | I/O | | PECI | Q31 PIN3 | PECI (Platform Environment Control Interface): A serial sideband interface to the processor, it is used primarily for thermal, power, and error management. | F.F. shutdown |
| | PROCHOT# | I/O | 1V | PROCHOT# | Q15 PIN3 | Processor Hot: PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC. | |
| | THERMTRIP# | O | 1.2V | THERMTRIP# | Q25 PIN1 | Thermal Trip: The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that<br>there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 130 °C.<br>This is signaled to the system by the THERMTRIP# signal. | |
| | CATERR# | O | | CATERR# | TP10 | Catastrophic Error: This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. | |
| Miscellaneous Signals | CFG[17:0] | I | | CFG[17:0] | | Configuration Signals | PCIEX16 graphic card can't display |
| | -H_SNB | | 1.8V | FC_x | R247 | FC signals are signals that are available for compatibility with other processors. | No Boot |
| | PMSYNC | I | | PM_SYNC | | Power Management Sync: A sideband signal to communicate power management status from the platform to the processor. | No Boot |
| | -SKTOCC | O | 0V | SKTOCC# | R257 | SKTOCC# (Socket Occupied) : This signal is pulled down directly (0 Ohms) on the processor package to the ground. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present. | CPU can't detect |
| PCI Express Graphics Interface | GRCOMP | I | 1.0V | PEG_ICOMPI | R24 | PCI Express* Input Current Compensation | PCIEX16 graphic card can't display |
| | GRCOMP | I | 1.0V | PEG_ICOMPO | R24 | PCI Express* Current Compensation | |
| | GRCOMP | I | 1.0V | PEG_RCOMPO | R24 | PCI Express* Resistance Compensation | |
| | EXP_A_RXP[15;0] | I | 0.6V | PEG_RX[15:0]<br>PEG_RX#[15:0]<br>PE_RX[3:0]1<br>PE_RX#[3:0]1 | PCIEX16 slot | PCI Express* Receive Differential Pair | |
| | EXP_A_TXP[15;0] | O | 0.6V | PEG_TX[15:0]<br>PEG_TX#[15:0]<br>PE_TX[3:0]1<br>PE_TX#[3:0]1 | C22~C83 / PCIEX16 slot | PCI Express* Transmit Differential Pair | |
| Test Access Points (TAP) Signals | ITPCLK<br>-ITPCLK | I | 100MHz | BCLK_ITP<br>BCLK_ITP# | Emulator | These signals are connected in parallel to the top side debug probe to enable debug capacities | No boot |
| | HPRDY# | I | 1.0V | PRDY# | RN6 | PRDY# is a processor output used by debug tools to determine processor debug readiness | No boot |
| | TCK | I | 1.0V | TCK | RN19 | Test Clock: This signal provides the clock input for the processor Test Bus | No boot |
| | TDI | I | 1.0V | TDI | RN6 | Test Data In: This signal transfers serial test data into the processor. | No boot |
| | TDO | O | 1.0V | TDO | RN6 | Test Data Out: This signal transfers serial test data out of the processor. | No boot |
| | TMS | I | 1.0V | TMS | RN6 | Test Mode Select: A JTAG specification support signal used by debug tools. | No boot |
| | TRST# | I | 1.0V | TRST# | RN19 | Test Reset: This signal resets the Test Access Port (TAP) logic.TRST# must be driven low during power on Reset. | No boot |
| System Memory Interface | SM_VREF | I | 0.75V | SM_VREF | R191,R193 | DDR3 Reference Voltage: This signal is used as a reference voltage to the DDR3 controller. | C1 |
| | VREF_DQA | O | 0.75V | VREF_DQA | TR27,28 | Memory Channel A DIMM DQ Voltage Reference: | C1 |
| | VREF_DQB | O | 0.75V | VREF_DQB | TR29,30 | Memory Channel B DIMM DQ Voltage Reference: | C1 |